

ZC3 BLOCK DIAGRAM

AMD K8/RX485/SB460 REV:B

BOM
VRAM@ ->(Samsung, Infineon, Hynix)
UC@ ->(ATMEL, SST)
MEMID@ ->(Samsung, Infineon, Hynix)
2@ ->Add second source

SYSTEM POWER
MAX1999

Page 44

CPU CORE(MAX8774)

Page 41

+1.2V/+1.5V/+2.5V

Page 42

+1.8V / VGA_CORE

Page 43,46

DISCHARGE CIRCUIT

Page 44

Clock GEN
ICS951462

Page 2

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
PCI 33MHz
REF 14MHz

R,G,B

CRT port

Page 26

LCD

LCD CONN

Page 25

TV-OUT

S-VIDEO

Page 25

TMDS

HDMI

Page 34

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
TI 7412	AD25	REQ0# / GNT0#	INTE# , F# , G#	PCICLK2
BCM5788M	AD20	REQ2# / GNT2#	INT#	PCICLK5

CPU THERMAL SENSOR
Page 13

AMD S1 Turion 64
(638 S1g1 socket)

Page 3,4,5,6

DDR II
533,667MHz

DDR II-SODIMM1

Page 7,8

DDR II-SODIMM2

Page 7,8

HyperTransport I/O BUS
LINK 16X16

NORTH BRIDGE
RX485
465 FCBGA

Page 9,10,11,12

PCIE 16X

ATI M56-P

Page 18,19,20,21,22,24

VRAM X4
(GDDR3 500MHZ)

Page 23

2X PCI-E 0,1

1X PCI-E 3

1X PCI-E 2

USB 2.0 * 1(USB5)

USB 2.0 * 4(USB0 ~ 3)

USB 2.0 * 1(USB6)

USB 2.0 * 1(USB7)

Primary IDE HDD
Page 35

SATA

Media bay CDROM
Page 35

ATA 66/100

A-LINK

SOUTH BRIDGE
SB460
549 BGA

Page 14,15,16,17

PCI/33MHz

Azalia

AUDIO CODEC
ALC883

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HP AMP

Page 37

SPK AMP

Page 37

HP/ SPDIF

Page 37

INT SPK

Page 37

Line-in & MIC

Page 37

MDC1.5 MODEM

Page 36

RJ11

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CARDBUS/1394/Card reader
TI 7412

Page 30,31

PCMCIA

Page 31

1394

Page 30

6 in 1 Cardreader

Page 31

Giga LAN
Broadcom BCM5788MG

Page 27

RJ45

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EZ4 Docking Connector

PCIE1~2 , Lan
Ser & Par Port
PS2 , VGA, DVI
SPDIF, SM BUS

Page 32

PCI-Express X 2

TV out / CRT

Switch

Page 25,26

Audio

Switch

Page 37

DVI

Switch

Page 34

10/100/1G

Switch

Page 28

USB0: M/B IO
USB1: M/B IO
USB2: D/B IO
USB3: D/B IO
USB4: D/B IO
USB5: NEW CARD
USB6: BLUETOOTH
USB7: CAMERA

SUPER I/O
PC87383

Page 38

Embedded Controller
NS 551

Page 39

FIR

Page 38

BIOS

Page 39

Keyboard

Page 40

Touchpad

Page 40

SWITCH & LED

Page 40

FAN

Page 13



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Quanta Computer Inc.

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Custom	BLOCK DIAGRAM	B2A
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PROCESSOR HYPERTRANSPORT INTERFACE

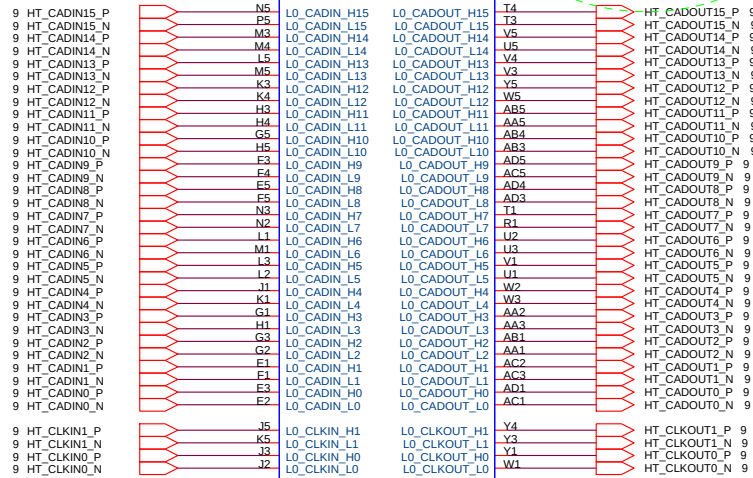
VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VLDT_RUN U43A

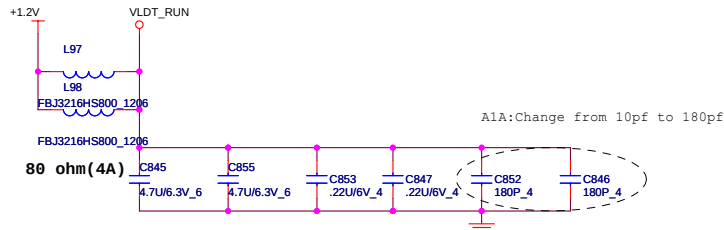
D4 VLDT_A3
D3 VLDT_A2
D2 VLDT_A1
D1 VLDT_A0

VLDT_B3
VLDT_B2
VLDT_B1
VLDT_B0

C495
4.7U/6.3V_6



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board

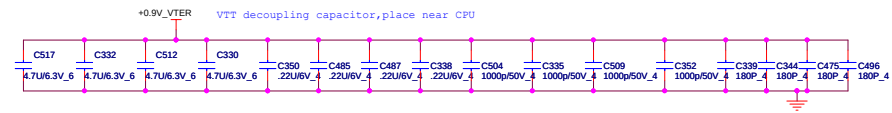
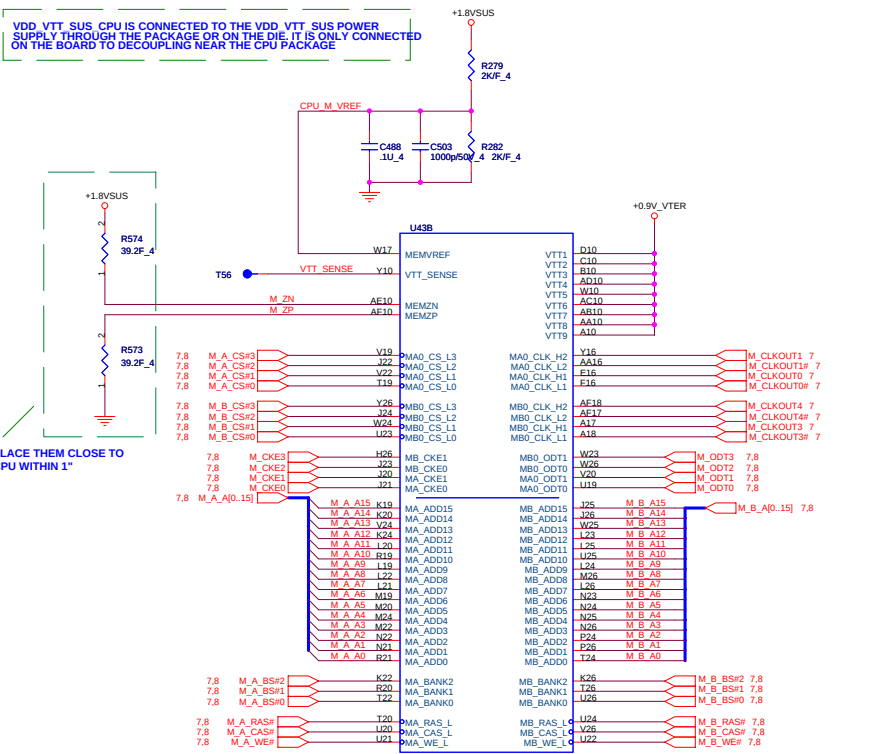


NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



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Quanta Computer Inc.

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	ATHLON64 HT I/F	1A
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DDR: DATA
Athlon 64 S1
Processor Socket

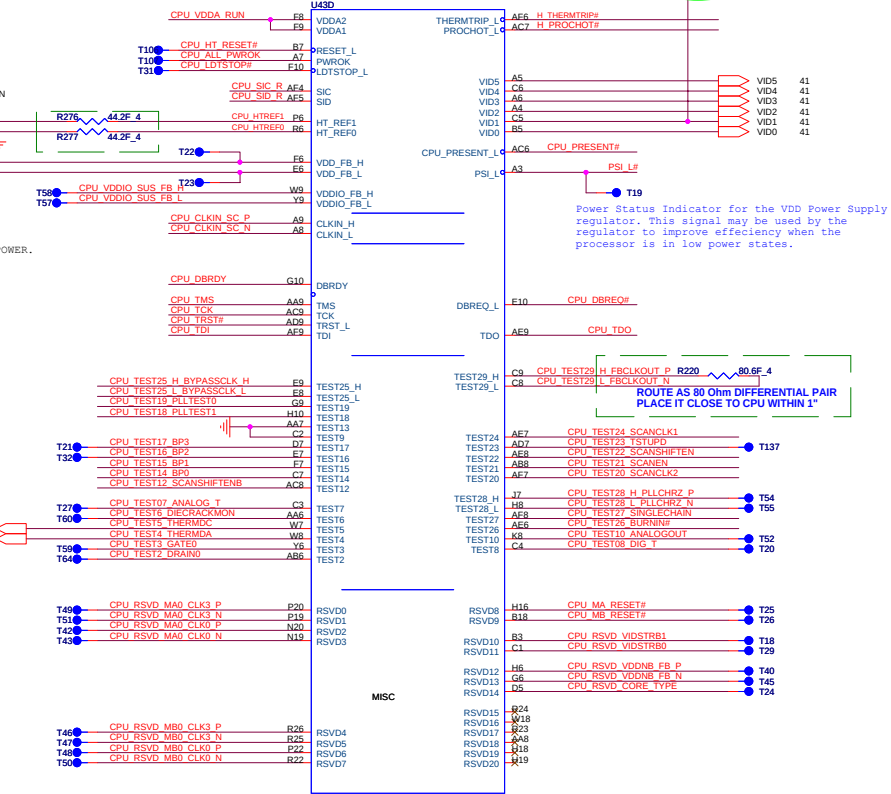
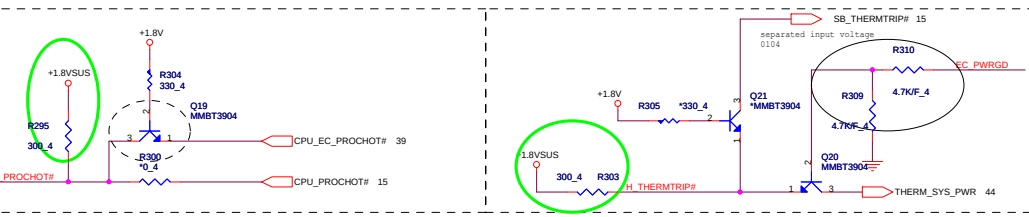
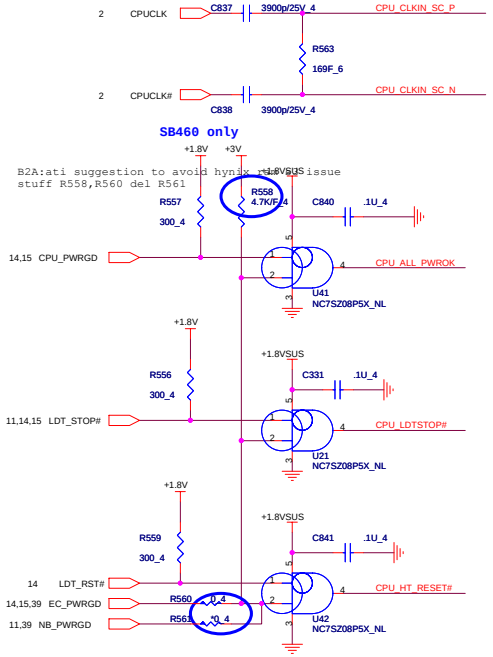
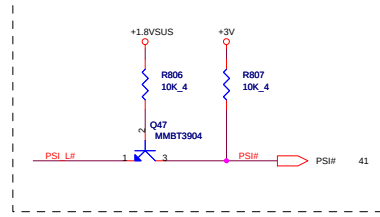
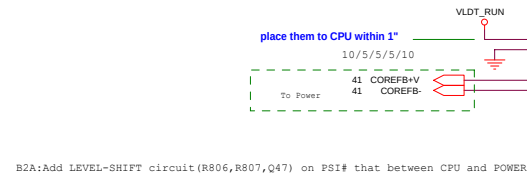
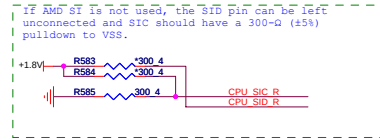
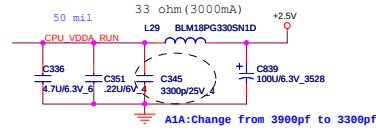
Top Section (M_B, M_A, M_D signals):

- M_B DMS0** (Pin 7) connects to **M_B DMS0** (Pin 7) and **M_B DMS0** (Pin 7).
- M_B DMS1** (Pin 8) connects to **M_B DMS1** (Pin 8) and **M_B DMS1** (Pin 8).
- M_B DMS2** (Pin 9) connects to **M_B DMS2** (Pin 9) and **M_B DMS2** (Pin 9).
- M_B DMS3** (Pin 10) connects to **M_B DMS3** (Pin 10) and **M_B DMS3** (Pin 10).
- M_B DMS4** (Pin 11) connects to **M_B DMS4** (Pin 11) and **M_B DMS4** (Pin 11).
- M_B DMS5** (Pin 12) connects to **M_B DMS5** (Pin 12) and **M_B DMS5** (Pin 12).
- M_B DMS6** (Pin 13) connects to **M_B DMS6** (Pin 13) and **M_B DMS6** (Pin 13).
- M_B DMS7** (Pin 14) connects to **M_B DMS7** (Pin 14) and **M_B DMS7** (Pin 14).
- M_B DMS8** (Pin 15) connects to **M_B DMS8** (Pin 15) and **M_B DMS8** (Pin 15).
- M_B DMS9** (Pin 16) connects to **M_B DMS9** (Pin 16) and **M_B DMS9** (Pin 16).
- M_B DMS10** (Pin 17) connects to **M_B DMS10** (Pin 17) and **M_B DMS10** (Pin 17).
- M_B DMS11** (Pin 18) connects to **M_B DMS11** (Pin 18) and **M_B DMS11** (Pin 18).
- M_B DMS12** (Pin 19) connects to **M_B DMS12** (Pin 19) and **M_B DMS12** (Pin 19).
- M_B DMS13** (Pin 20) connects to **M_B DMS13** (Pin 20) and **M_B DMS13** (Pin 20).
- M_B DMS14** (Pin 21) connects to **M_B DMS14** (Pin 21) and **M_B DMS14** (Pin 21).
- M_B DMS15** (Pin 22) connects to **M_B DMS15** (Pin 22) and **M_B DMS15** (Pin 22).
- M_B DMS16** (Pin 23) connects to **M_B DMS16** (Pin 23) and **M_B DMS16** (Pin 23).
- M_B DMS17** (Pin 24) connects to **M_B DMS17** (Pin 24) and **M_B DMS17** (Pin 24).
- M_B DMS18** (Pin 25) connects to **M_B DMS18** (Pin 25) and **M_B DMS18** (Pin 25).
- M_B DMS19** (Pin 26) connects to **M_B DMS19** (Pin 26) and **M_B DMS19** (Pin 26).
- M_B DMS20** (Pin 27) connects to **M_B DMS20** (Pin 27) and **M_B DMS20** (Pin 27).
- M_B DMS21** (Pin 28) connects to **M_B DMS21** (Pin 28) and **M_B DMS21** (Pin 28).
- M_B DMS22** (Pin 29) connects to **M_B DMS22** (Pin 29) and **M_B DMS22** (Pin 29).
- M_B DMS23** (Pin 30) connects to **M_B DMS23** (Pin 30) and **M_B DMS23** (Pin 30).
- M_B DMS24** (Pin 31) connects to **M_B DMS24** (Pin 31) and **M_B DMS24** (Pin 31).
- M_B DMS25** (Pin 32) connects to **M_B DMS25** (Pin 32) and **M_B DMS25** (Pin 32).
- M_B DMS26** (Pin 33) connects to **M_B DMS26** (Pin 33) and **M_B DMS26** (Pin 33).
- M_B DMS27** (Pin 34) connects to **M_B DMS27** (Pin 34) and **M_B DMS27** (Pin 34).
- M_B DMS28** (Pin 35) connects to **M_B DMS28** (Pin 35) and **M_B DMS28** (Pin 35).
- M_B DMS29** (Pin 36) connects to **M_B DMS29** (Pin 36) and **M_B DMS29** (Pin 36).
- M_B DMS30** (Pin 37) connects to **M_B DMS30** (Pin 37) and **M_B DMS30** (Pin 37).
- M_B DMS31** (Pin 38) connects to **M_B DMS31** (Pin 38) and **M_B DMS31** (Pin 38).
- M_B DMS32** (Pin 39) connects to **M_B DMS32** (Pin 39) and **M_B DMS32** (Pin 39).
- M_B DMS33** (Pin 40) connects to **M_B DMS33** (Pin 40) and **M_B DMS33** (Pin 40).
- M_B DMS34** (Pin 41) connects to **M_B DMS34** (Pin 41) and **M_B DMS34** (Pin 41).
- M_B DMS35** (Pin 42) connects to **M_B DMS35** (Pin 42) and **M_B DMS35** (Pin 42).
- M_B DMS36** (Pin 43) connects to **M_B DMS36** (Pin 43) and **M_B DMS36** (Pin 43).
- M_B DMS37** (Pin 44) connects to **M_B DMS37** (Pin 44) and **M_B DMS37** (Pin 44).
- M_B DMS38** (Pin 45) connects to **M_B DMS38** (Pin 45) and **M_B DMS38** (Pin 45).
- M_B DMS39** (Pin 46) connects to **M_B DMS39** (Pin 46) and **M_B DMS39** (Pin 46).
- M_B DMS40** (Pin 47) connects to **M_B DMS40** (Pin 47) and **M_B DMS40** (Pin 47).
- M_B DMS41** (Pin 48) connects to **M_B DMS41** (Pin 48) and **M_B DMS41** (Pin 48).
- M_B DMS42** (Pin 49) connects to **M_B DMS42** (Pin 49) and **M_B DMS42** (Pin 49).
- M_B DMS43** (Pin 50) connects to **M_B DMS43** (Pin 50) and **M_B DMS43** (Pin 50).
- M_B DMS44** (Pin 51) connects to **M_B DMS44** (Pin 51) and **M_B DMS44** (Pin 51).
- M_B DMS45** (Pin 52) connects to **M_B DMS45** (Pin 52) and **M_B DMS45** (Pin 52).
- M_B DMS46** (Pin 53) connects to **M_B DMS46** (Pin 53) and **M_B DMS46** (Pin 53).
- M_B DMS47** (Pin 54) connects to **M_B DMS47** (Pin 54) and **M_B DMS47** (Pin 54).
- M_B DMS48** (Pin 55) connects to **M_B DMS48** (Pin 55) and **M_B DMS48** (Pin 55).
- M_B DMS49** (Pin 56) connects to **M_B DMS49** (Pin 56) and **M_B DMS49** (Pin 56).
- M_B DMS50** (Pin 57) connects to **M_B DMS50** (Pin 57) and **M_B DMS50** (Pin 57).
- M_B DMS51** (Pin 58) connects to **M_B DMS51** (Pin 58) and **M_B DMS51** (Pin 58).
- M_B DMS52** (Pin 59) connects to **M_B DMS52** (Pin 59) and **M_B DMS52** (Pin 59).
- M_B DMS53** (Pin 60) connects to **M_B DMS53** (Pin 60) and **M_B DMS53** (Pin 60).
- M_B DMS54** (Pin 61) connects to **M_B DMS54** (Pin 61) and **M_B DMS54** (Pin 61).
- M_B DMS55** (Pin 62) connects to **M_B DMS55** (Pin 62) and **M_B DMS55** (Pin 62).
- M_B DMS56** (Pin 63) connects to **M_B DMS56** (Pin 63) and **M_B DMS56** (Pin 63).
- M_B DMS57** (Pin 64) connects to **M_B DMS57** (Pin 64) and **M_B DMS57** (Pin 64).
- M_B DMS58** (Pin 65) connects to **M_B DMS58** (Pin 65) and **M_B DMS58** (Pin 65).
- M_B DMS59** (Pin 66) connects to **M_B DMS59** (Pin 66) and **M_B DMS59** (Pin 66).
- M_B DMS60** (Pin 67) connects to **M_B DMS60** (Pin 67) and **M_B DMS60** (Pin 67).
- M_B DMS61** (Pin 68) connects to **M_B DMS61** (Pin 68) and **M_B DMS61** (Pin 68).
- M_B DMS62** (Pin 69) connects to **M_B DMS62** (Pin 69) and **M_B DMS62** (Pin 69).
- M_B DMS63** (Pin 70) connects to **M_B DMS63** (Pin 70) and **M_B DMS63** (Pin 70).
- M_B DMS64** (Pin 71) connects to **M_B DMS64** (Pin 71) and **M_B DMS64** (Pin 71).
- M_B DMS65** (Pin 72) connects to **M_B DMS65** (Pin 72) and **M_B DMS65** (Pin 72).
- M_B DMS66** (Pin 73) connects to **M_B DMS66** (Pin 73) and **M_B DMS66** (Pin 73).
- M_B DMS67** (Pin 74) connects to **M_B DMS67** (Pin 74) and **M_B DMS67** (Pin 74).
- M_B DMS68** (Pin 75) connects to **M_B DMS68** (Pin 75) and **M_B DMS68** (Pin 75).
- M_B DMS69** (

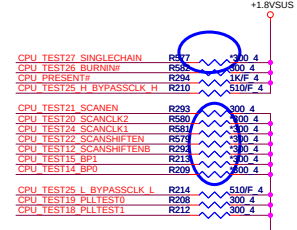
ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

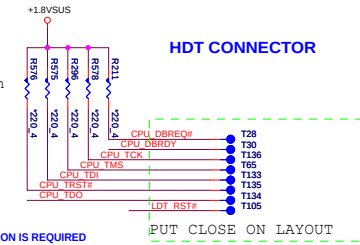


B2A: AMD suggestion not stuff
R577, R580, R581, R579, R292, R213, R209



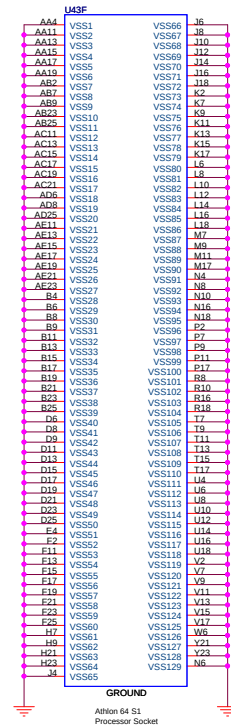
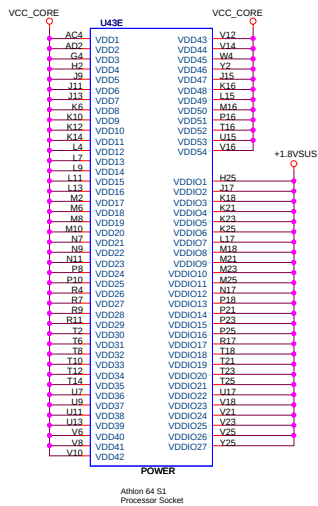
IF no use which Net
need pull-up or down

NOTE: HDT TERMINATION IS REQUIRED
FOR REV. Ax SILICON ONLY.

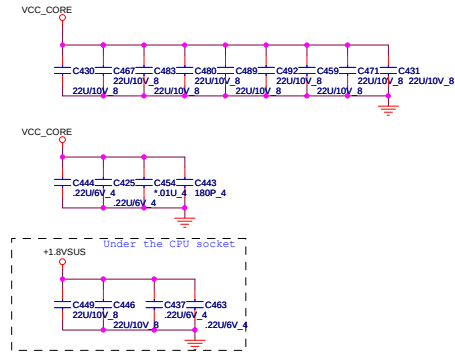


HDT CONNECTOR

PUT CLOSE ON LAYOUT

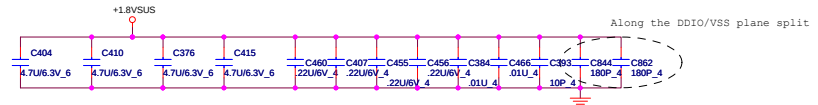


BOTTOMSIDE DECOUPLING

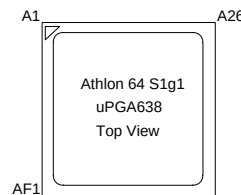


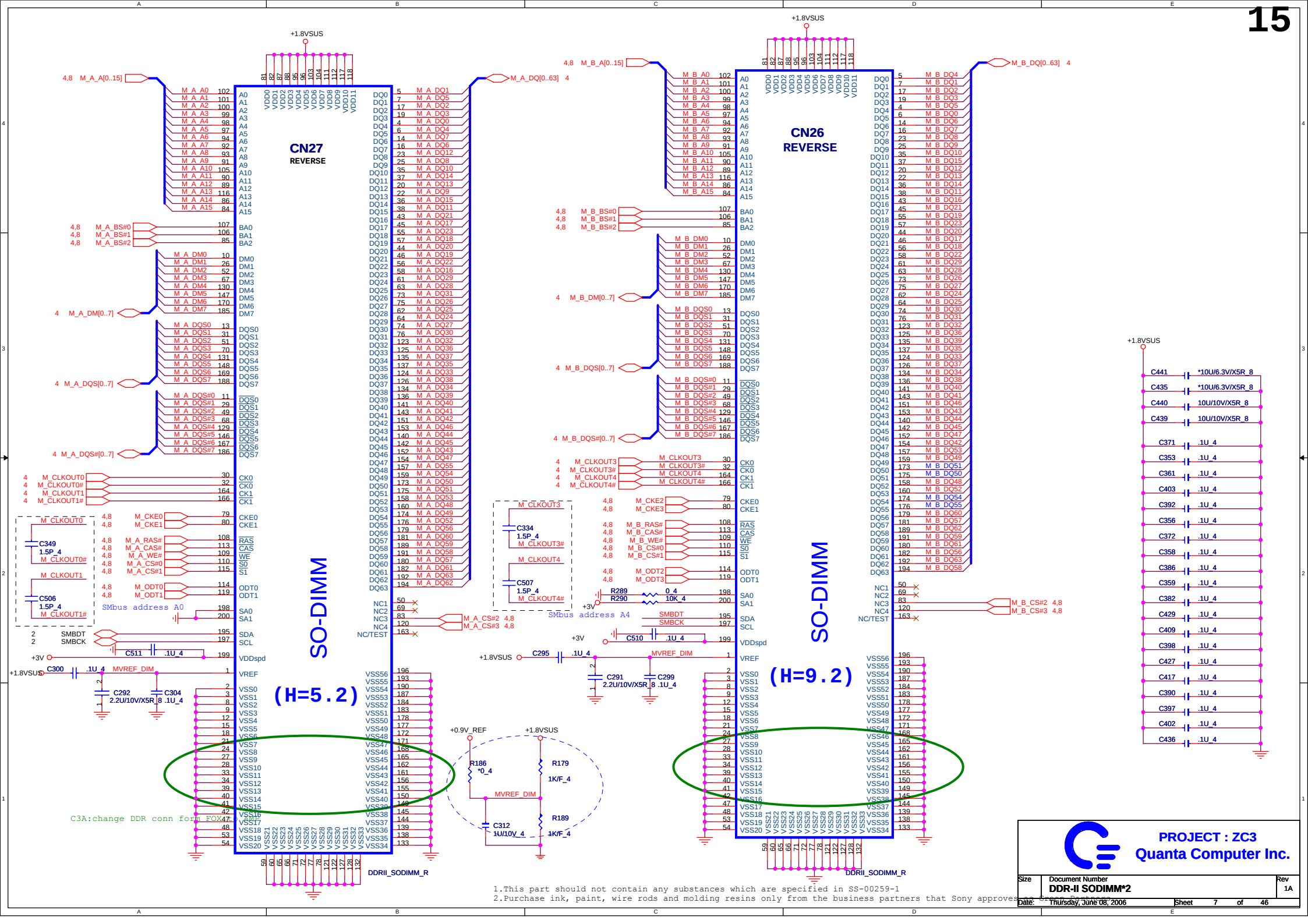
DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE

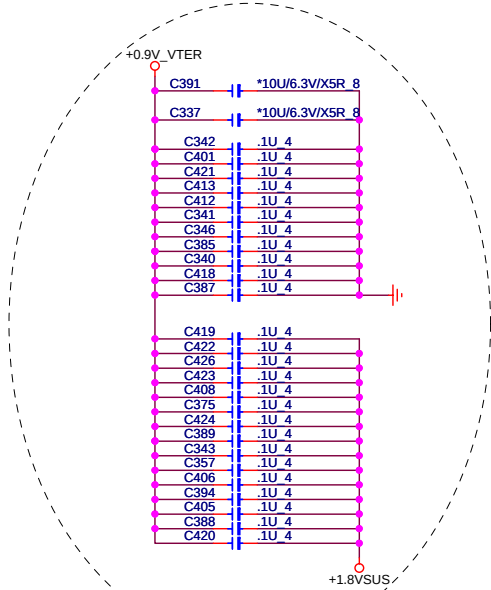


PROCESSOR POWER AND GROUND



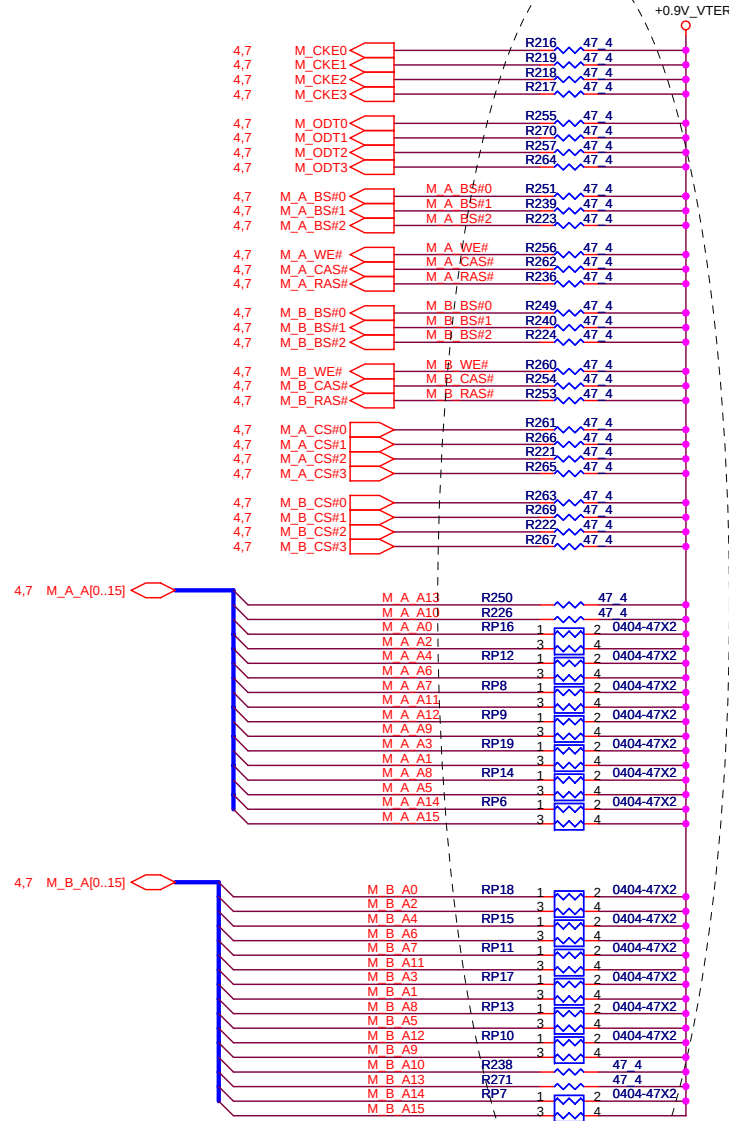


VTT is decoupled to VDDIO,VTT is decoupled to VSS



decoupling capacitors from VTT (+0.9V_VTER) to VDDIO (+1.8VSUS). Which is (1) decoupling capacitor for every (4) signals terminated to VTT

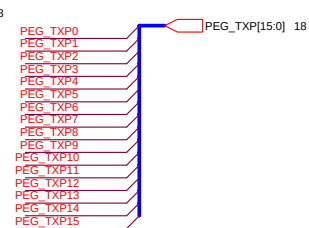
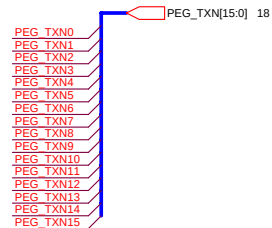
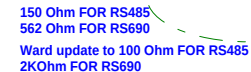
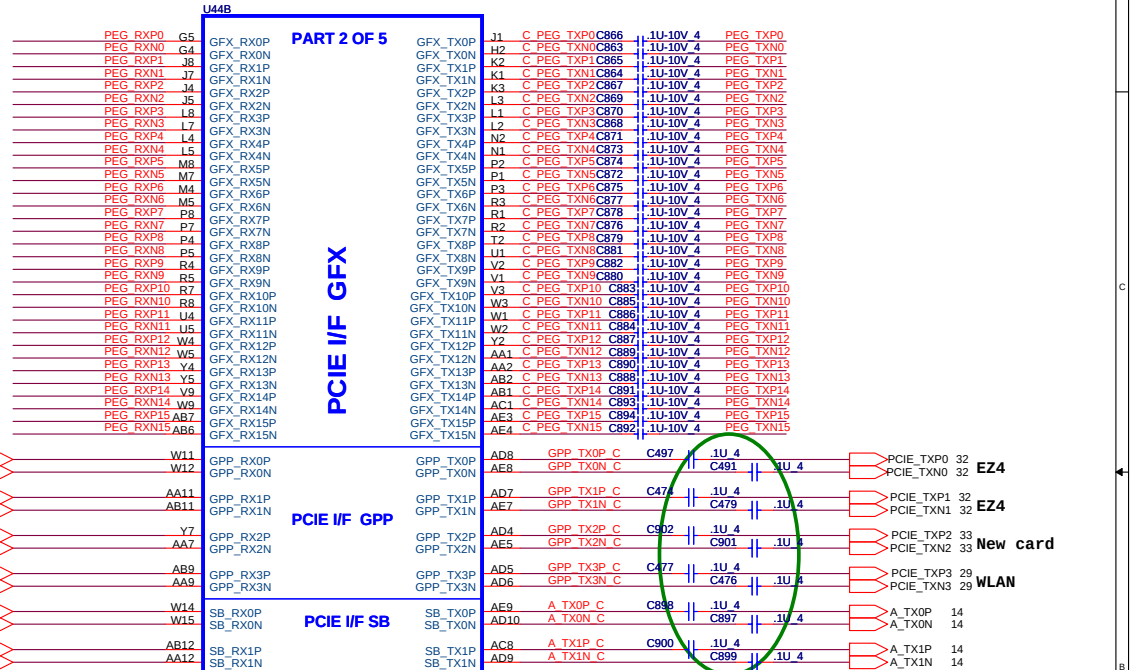
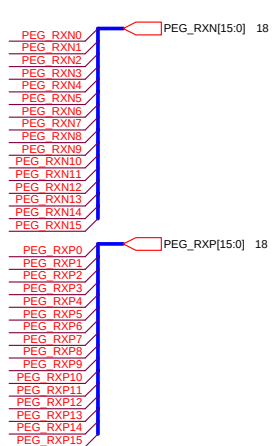
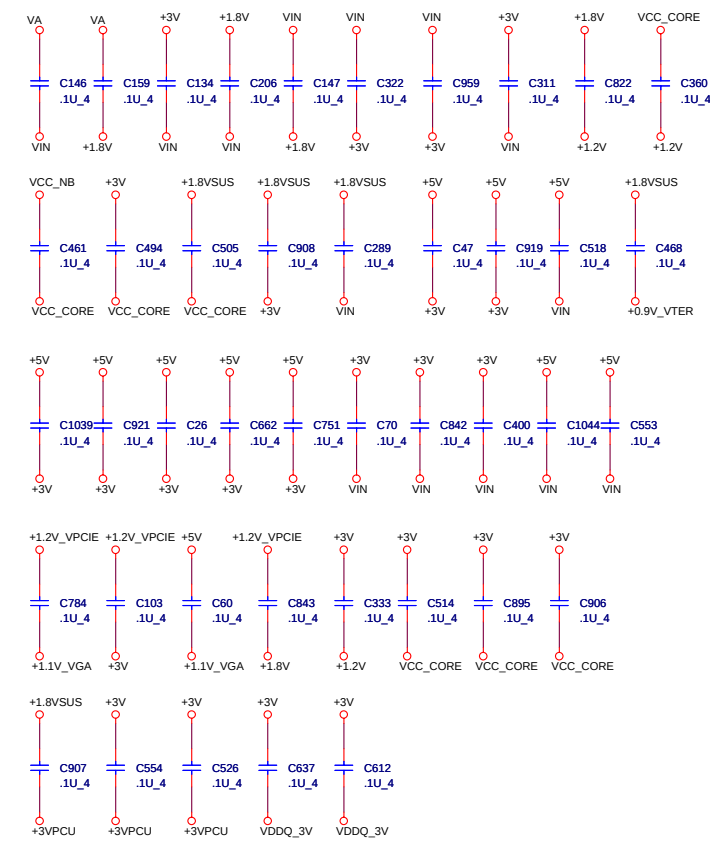
AlA:Change RTT termination from 56 to 47 ohm



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	DDR-II TERMINATION	1A
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Stiching capacitor

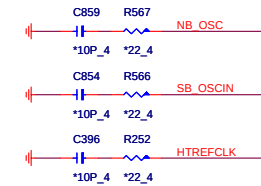
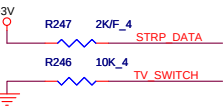
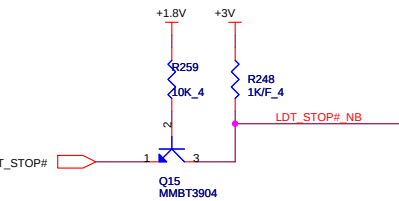
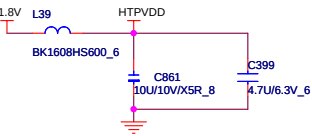
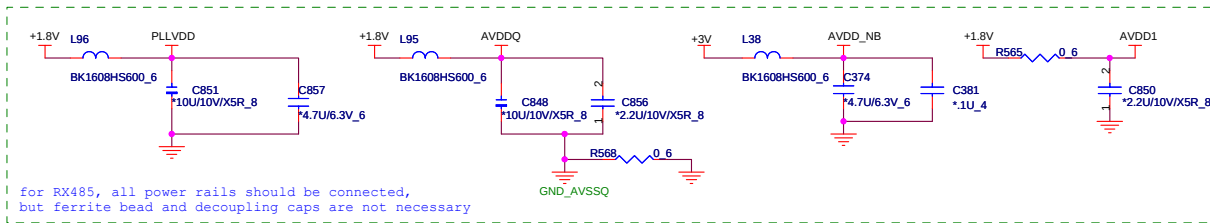


**Place these caps
close to connector**



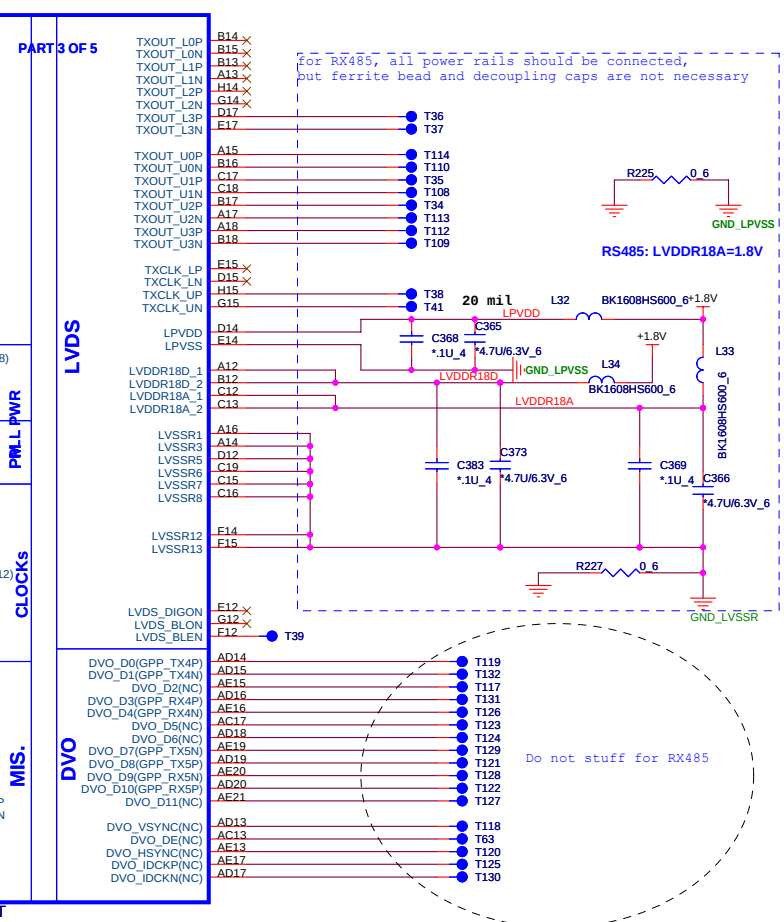
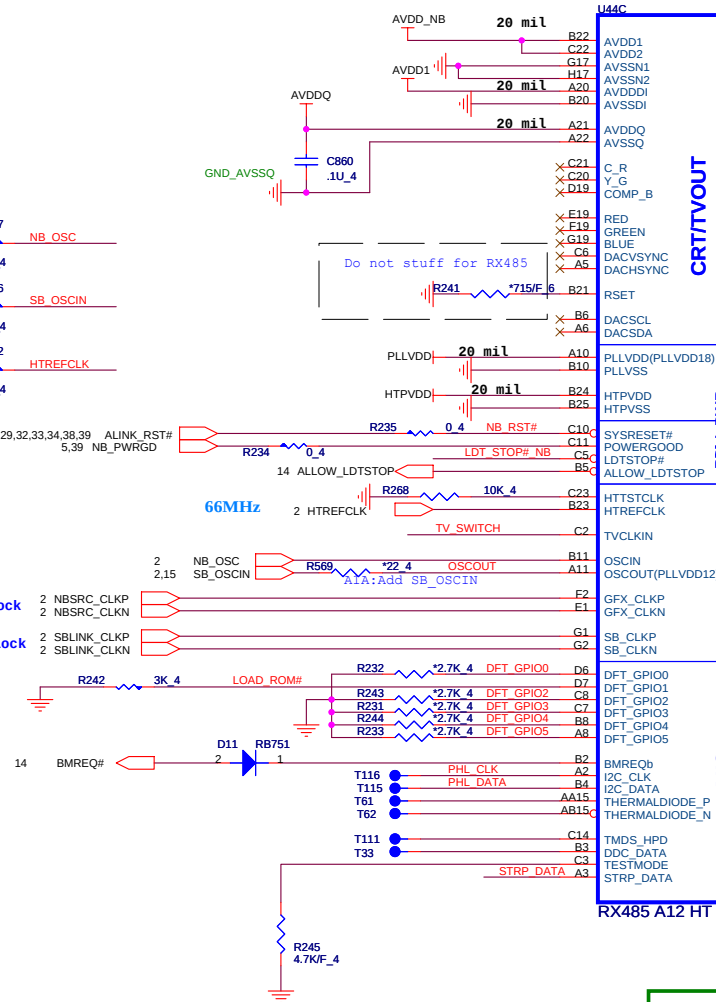
PROJECT : ZC3
Quanta Computer Inc.

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Date:	Thursdav, June 08, 2006	Sheet 10 of 46



PCI-E graphic clock
A-Link clock

LOAD_ROM#: LOAD ROM STRAP ENABLE
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



RX485 A12 HT

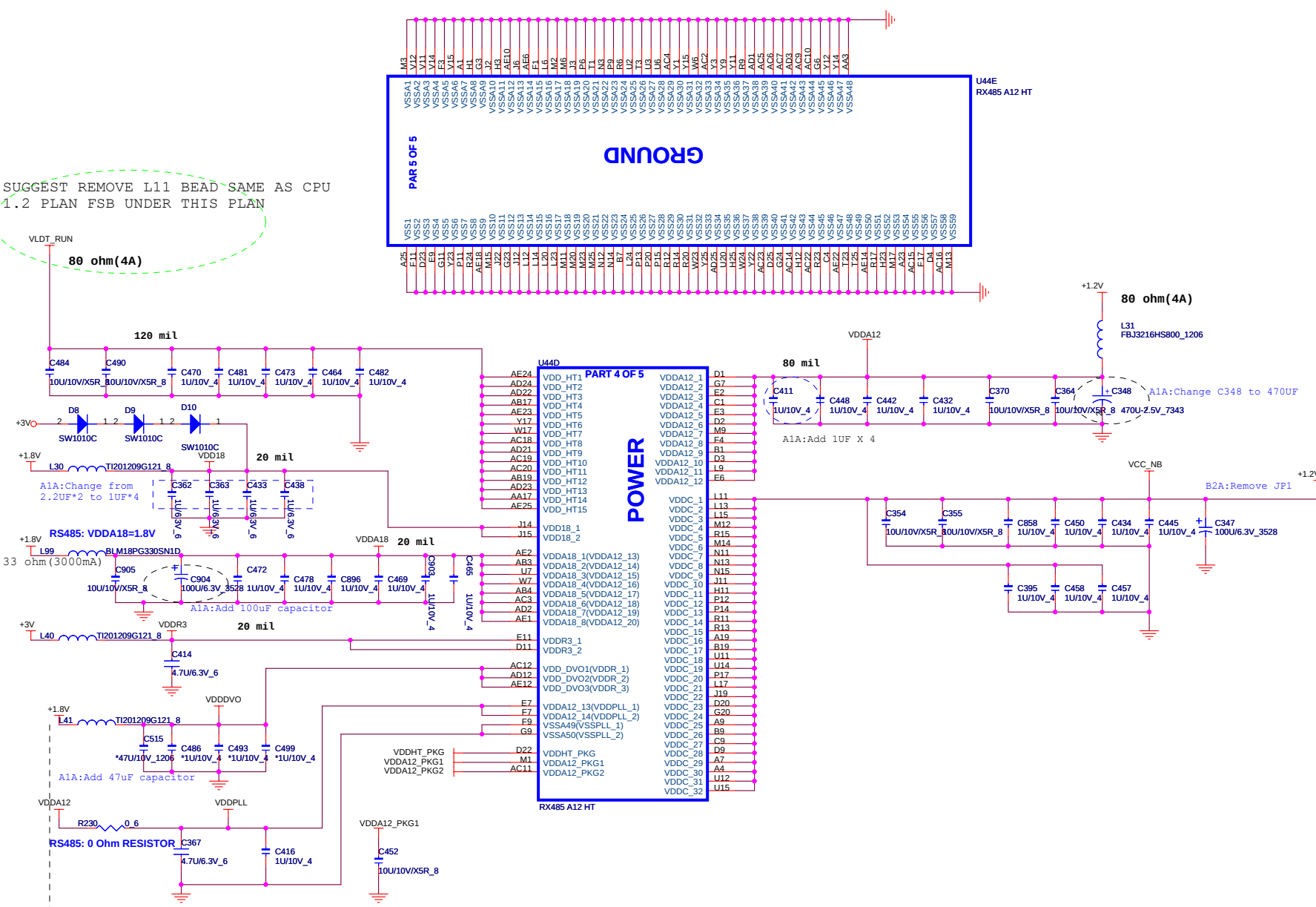
	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P



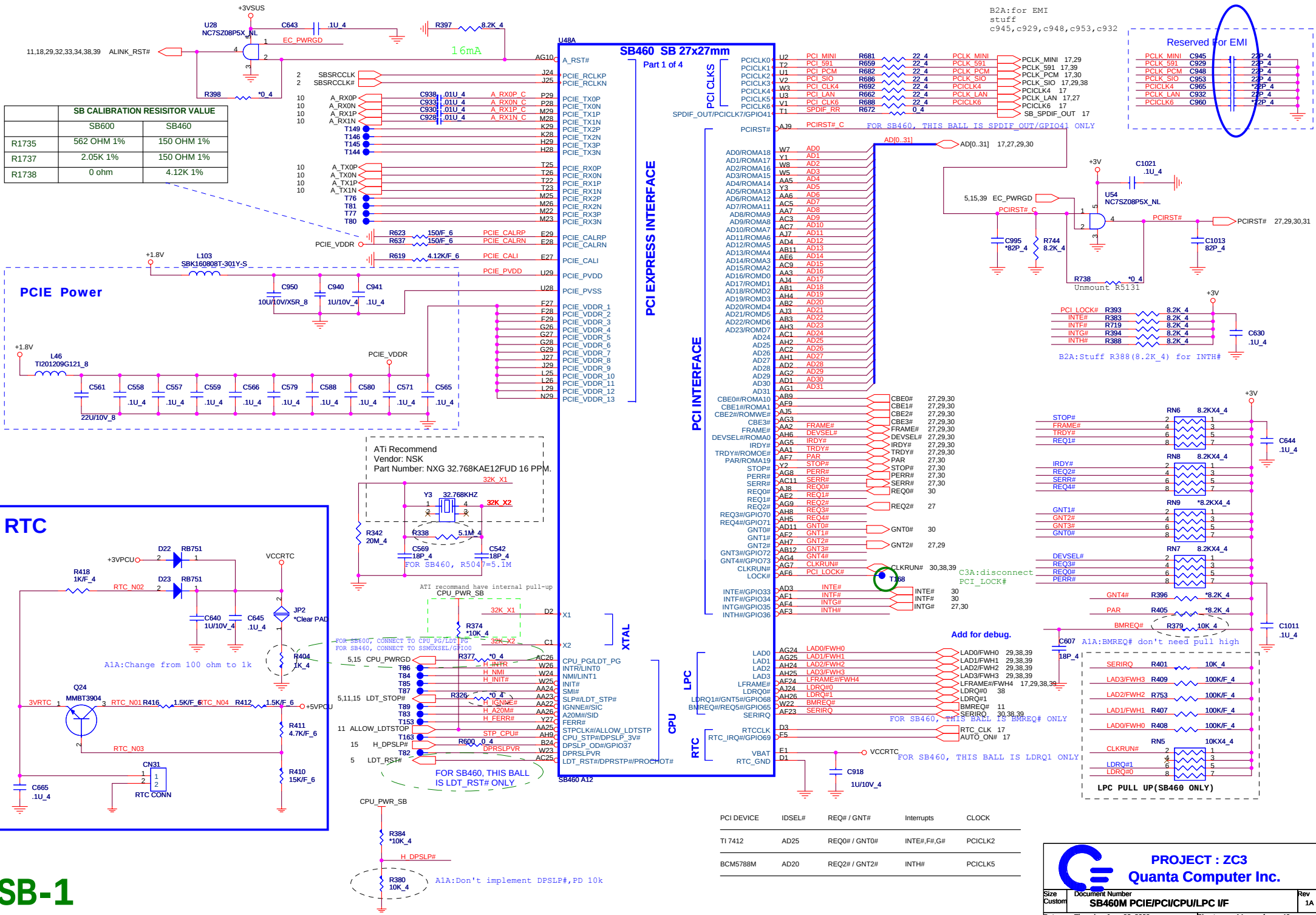
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Quanta Computer Inc.

Size	Document Number	Rev
	RS485-SYSTEM I/F & CLKGEN	1A
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SUGGEST REMOVE L11 BEAD-SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN



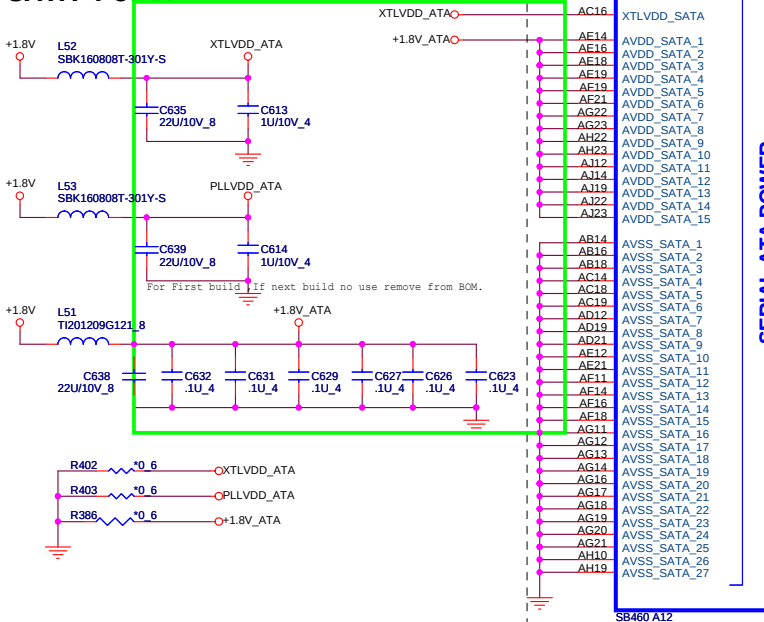
NB RS485 POWER STATES						
Power	Signal	S0	S1	S3	S4/S5	G3
VDDHT		ON	ON	OFF	OFF	OFF
VDDR		ON	ON	OFF	OFF	OFF
VDD18		ON	ON	OFF	OFF	OFF
VDDC		ON	ON	OFF	OFF	OFF
VDDA18		ON	ON	OFF	OFF	OFF
VDDA12		ON	ON	OFF	OFF	OFF
AVDD		ON	ON	OFF	OFF	OFF
AVDDDI		ON	ON	OFF	OFF	OFF
PLLVD		ON	ON	OFF	OFF	OFF
HTPVDD		ON	ON	OFF	OFF	OFF
VDDR3		ON	ON	OFF	OFF	OFF
LPVDD		ON	ON	OFF	OFF	OFF
LVDDR18D		ON	ON	OFF	OFF	OFF
LVDDR18A		ON	ON	OFF	OFF	OFF



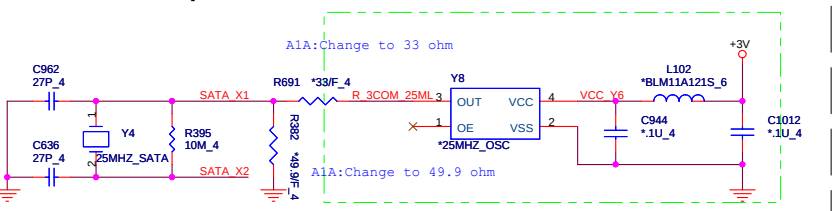
Part 2 of 4



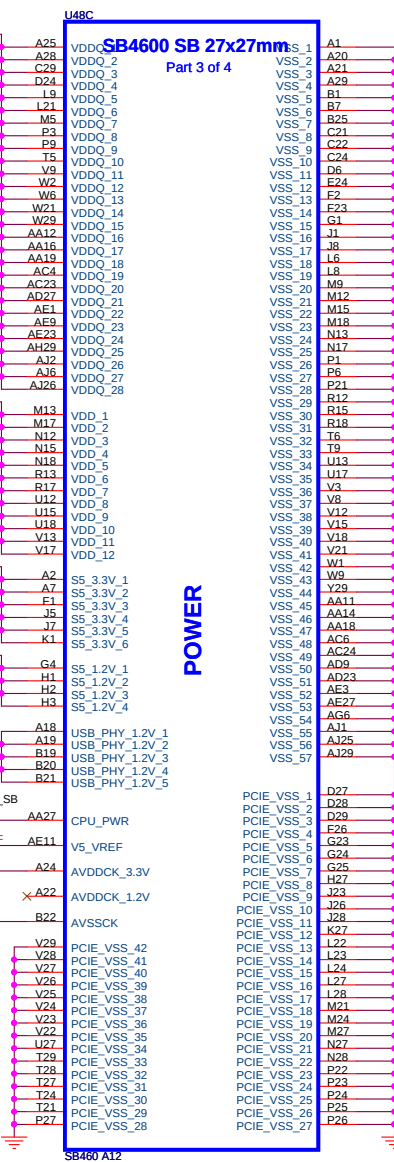
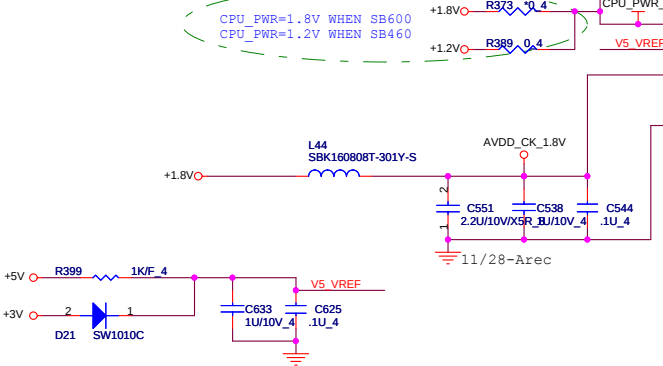
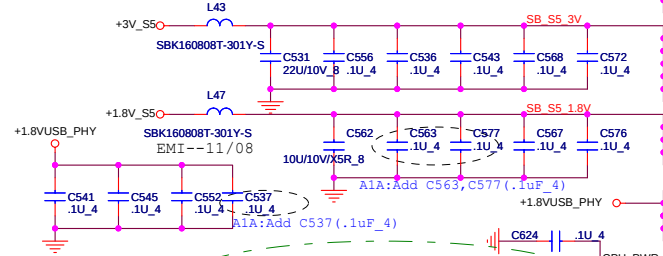
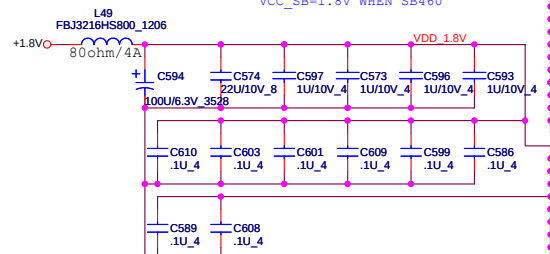
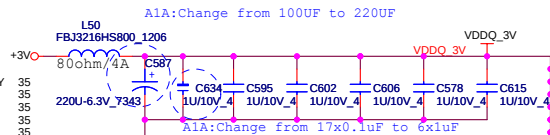
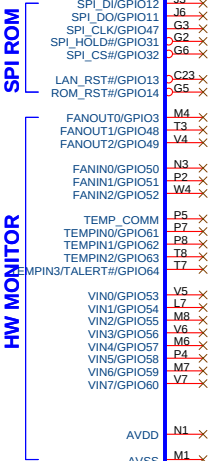
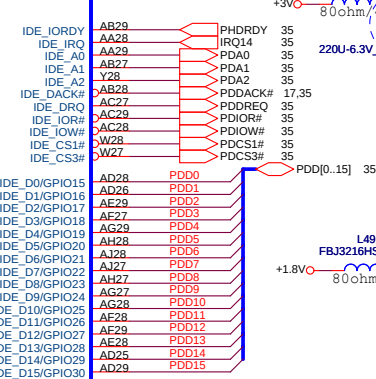
SATA Power



SATA clock Option



B2A:Remove R382,R691,Y8,C944,C1012,L102 for SATA clock



PROJECT : ZC3

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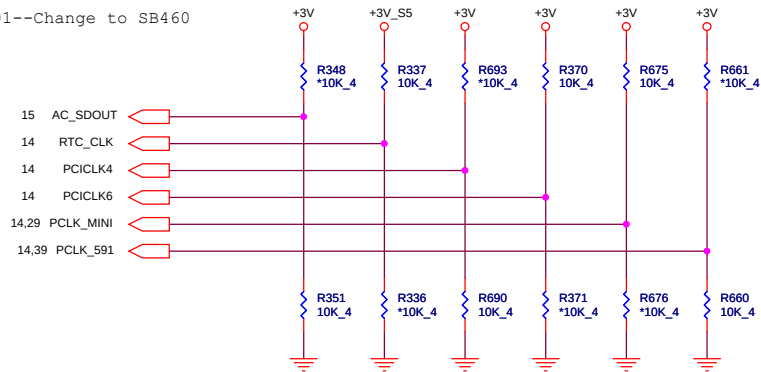
Size Custom Document Number **SB450M HDD/POWER/DECOUPLING**

Date: Thursday, June 08, 2006 Sheet 16 of 46

	1
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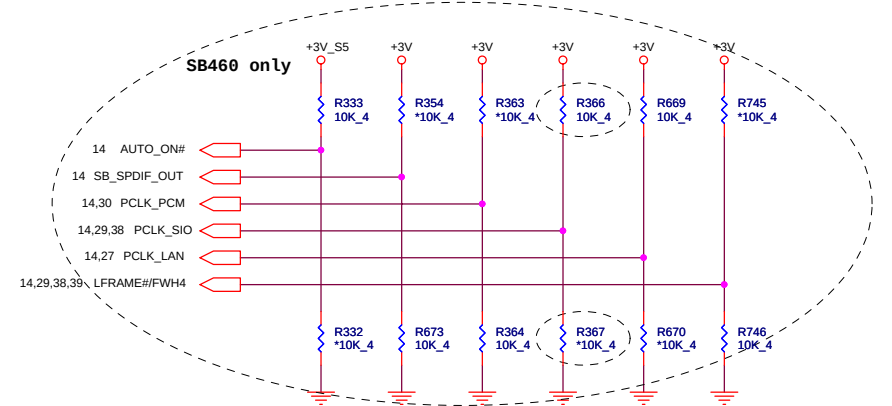
Rev

Edison-11/01--Change to SB460



REQUIRED STRAPS

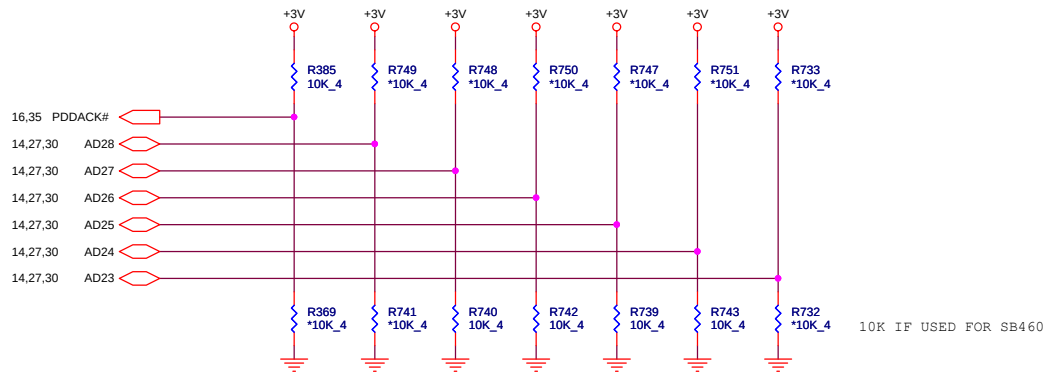
				PCLK_MINI PCLK_591	
PULL HIGH	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT



A1A:USB PHY POWERDOWN DISABLE

PULL HIGH	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON DEFAULT	SPDIF_OUT SIO 24MHz	PCI_CLK2 XTAL MODE NOT SUPPORTED	PCI_CLK3 USB PHY POWERDOWN DISABLE DEFAULT	PCI_CLK5 PCIE_CM_SET LOW DEFAULT	LFRAME# ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

SB460 only SB600 only

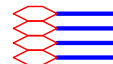
**PROJECT : ZC3**
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
SB460M STRAPS		
Date: Thursday, June 08, 2006	Sheet 17 of 46	

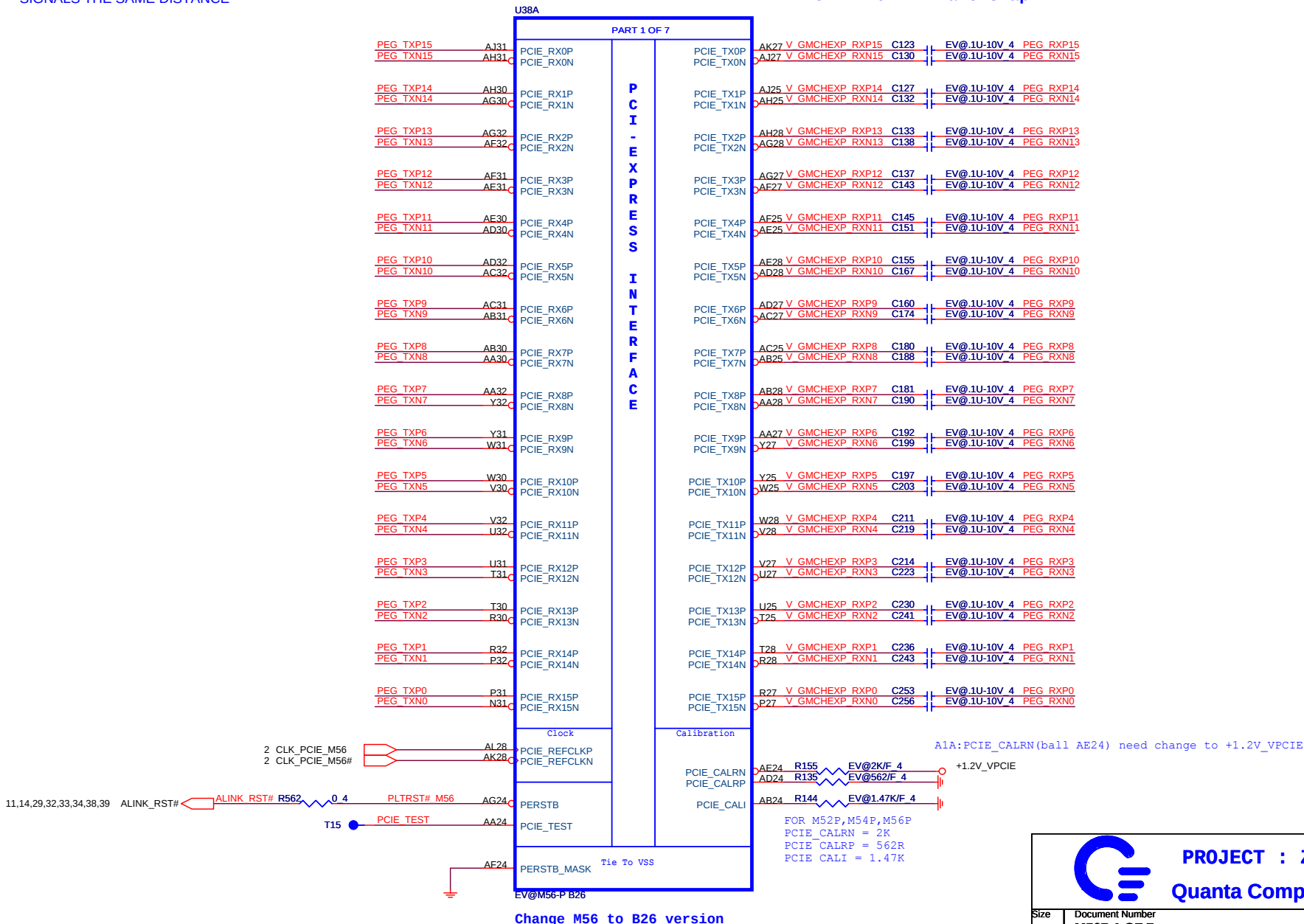
SB-4

PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

10 PEG_RXP[15:0]
10 PEG_RXN[15:0]
10 PEG_TXP[15:0]
10 PEG_TXN[15:0]



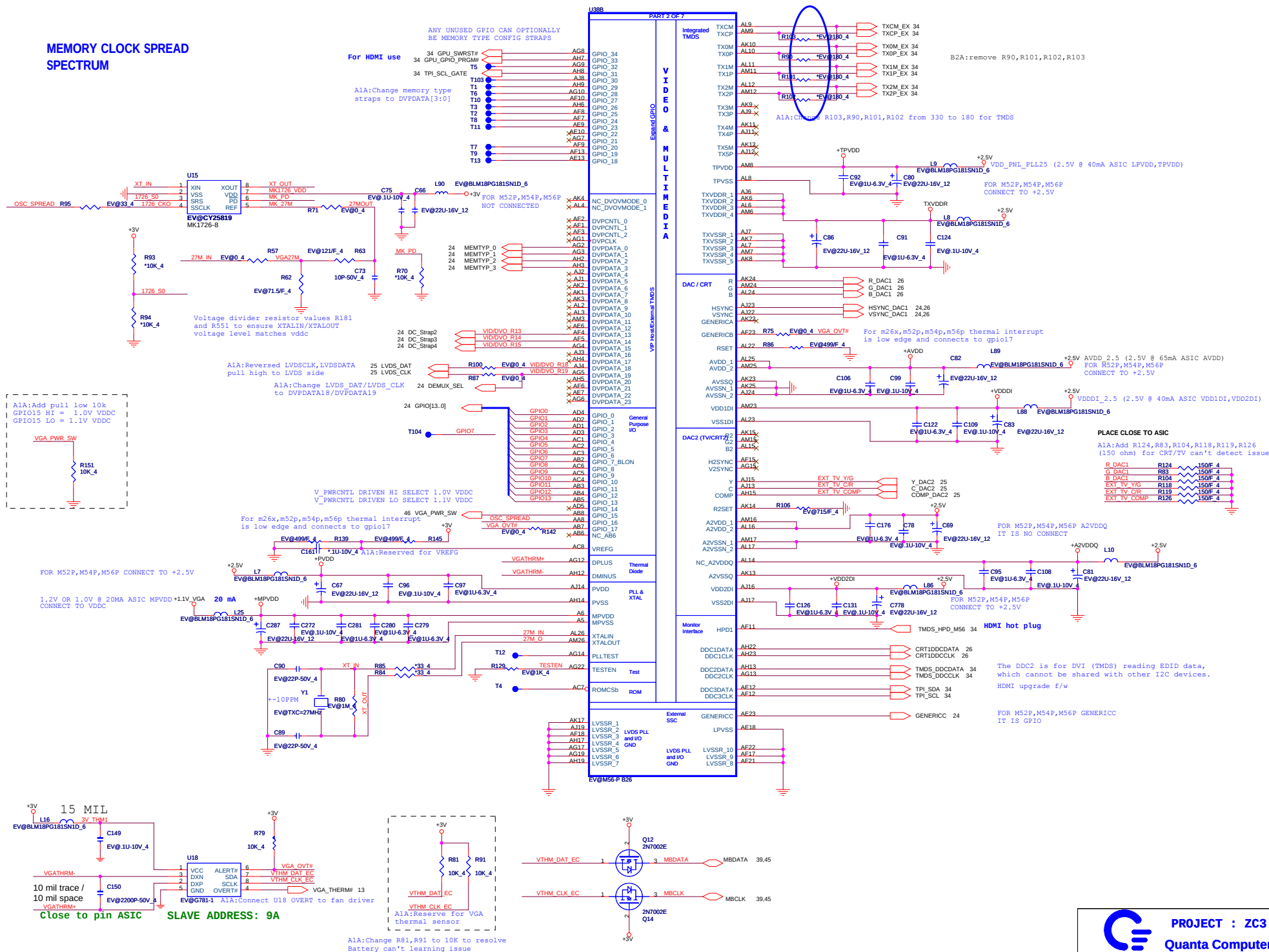
A1A:PCI-E 16X LAN are Swap



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Size	Document Number	Rev
	M56P 1 OF 7	1A
Date:	Thursday, June 08, 2006	Sheet 18 of 46

MEMORY CLOCK SPREAD SPECTRUM



VGA_MEM_IO

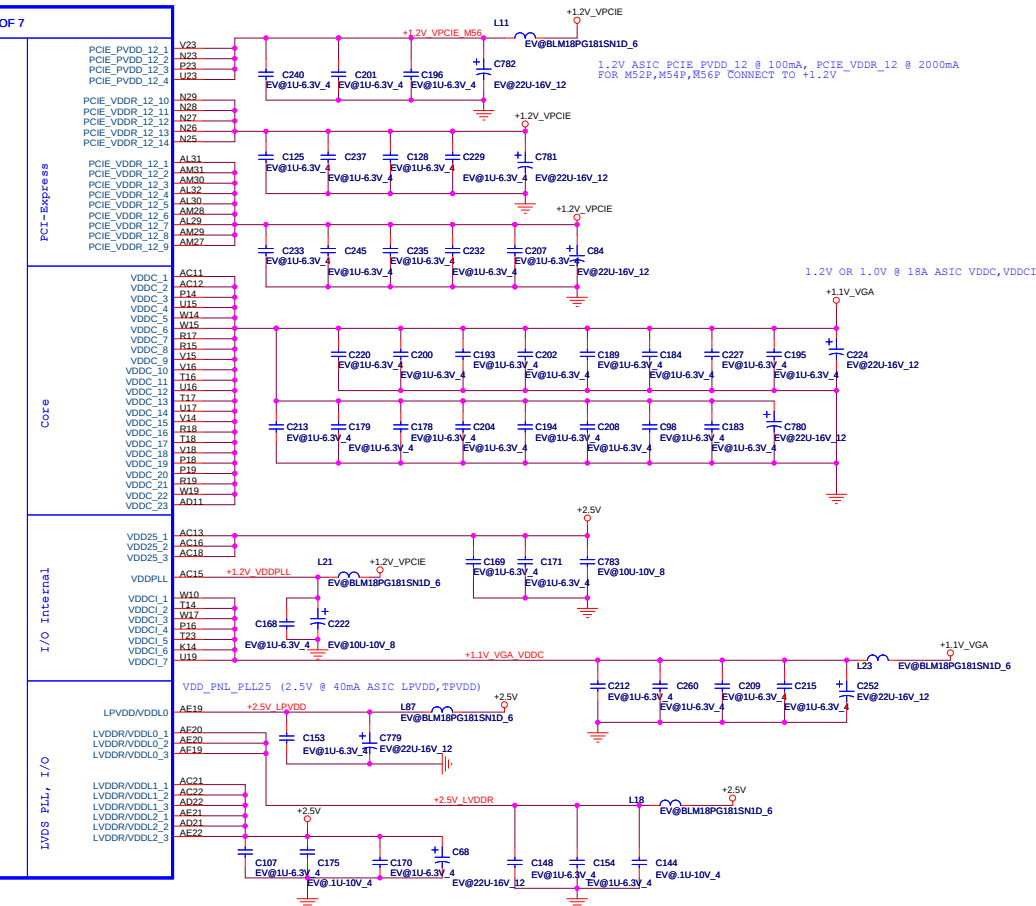
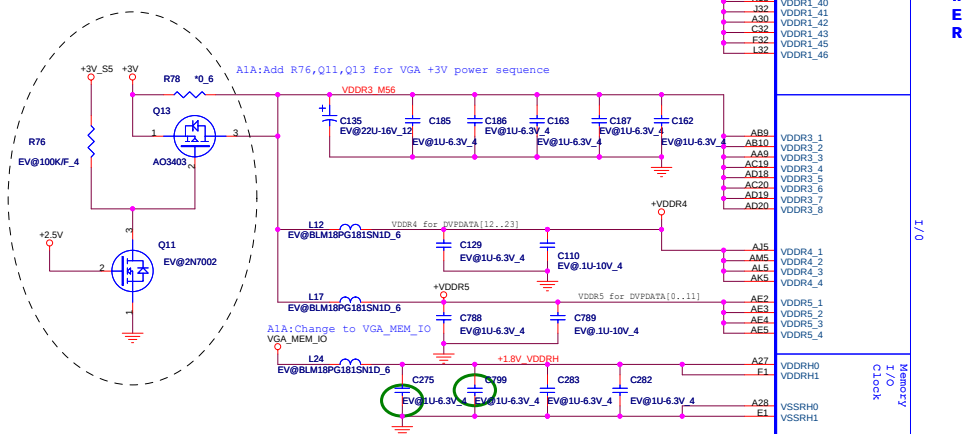
A1A:Change to VGA_MEM_IO

C374:change footprint form c0402-c to c0402

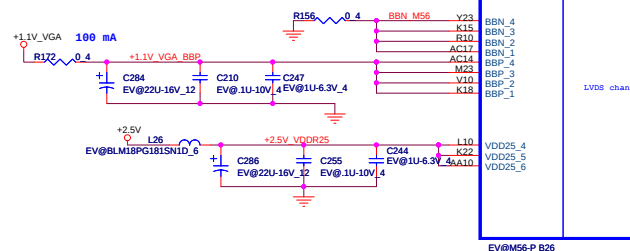
Part 5

Memory IO

C1 VDDR1_1
C2 VDDR1_2
C3 VDDR1_3
C4 VDDR1_4
C5 VDDR1_5
C6 VDDR1_6
C7 VDDR1_7
C8 VDDR1_8
C9 VDDR1_9
C10 VDDR1_10
C11 VDDR1_11
C12 VDDR1_12
C13 VDDR1_13
C14 VDDR1_14
C15 VDDR1_15
C16 VDDR1_16
C17 VDDR1_17
C18 VDDR1_18
C19 VDDR1_19
C20 VDDR1_20
C21 VDDR1_21
C22 VDDR1_22
C23 VDDR1_23
C24 VDDR1_24
C25 VDDR1_25
C26 VDDR1_26
C27 VDDR1_27
C28 VDDR1_28
C29 VDDR1_29
C30 VDDR1_30
C31 VDDR1_31
C32 VDDR1_32

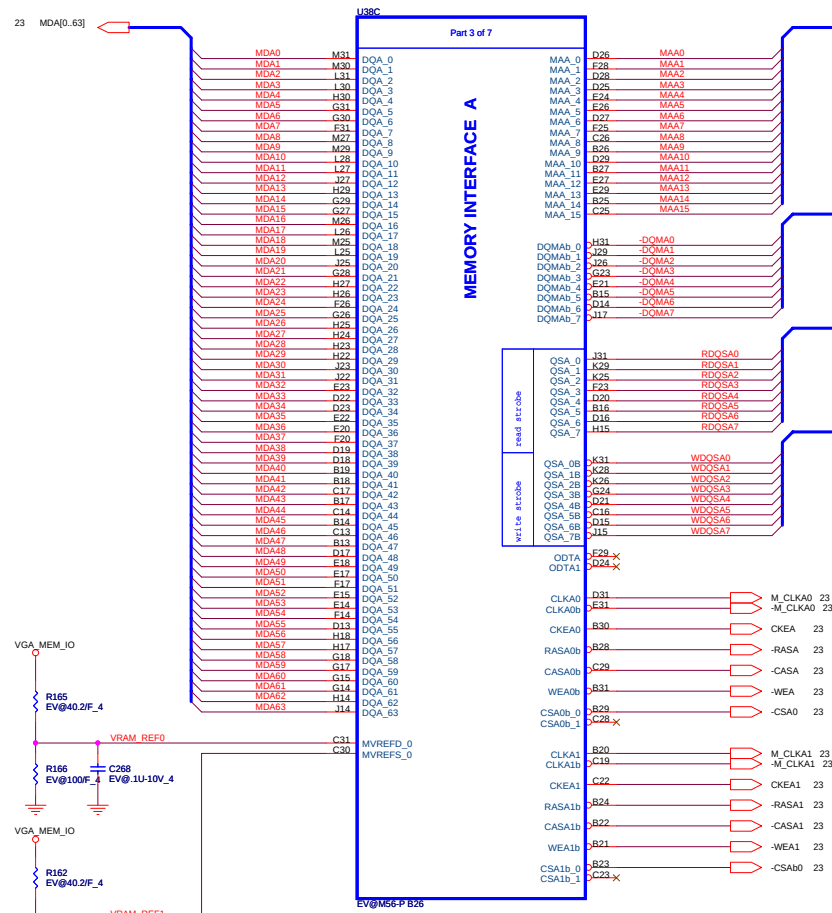


Pin	Signal	Direction	Notes
AD12	LVD5_BLOW	25	
AE11	LVD5_DIGNON	25	
AD23	Panel power(LCDVCC)_control		GENERIDC->FOR M56P IT IS A BACK BIAS REGULATOR CONTROL
AJ21	TXUCLKOUT+	25	
AK21	TXUCLKOUT-	25	
AH21	TXUOUT2+	25	
AG21	TXUOUT2-	25	
AG20	TXUOUT1+	25	
AH20	TXUOUT1-	25	
AK20	TXUOUT0+	25	
AJ20	TXUOUT0-	25	
AG18	TXUOUT0+	25	
AH18	TXUOUT0-	25	
AK19	TXLOUT0-	25	
AL19	TXLOUT0+	25	
AL20	TXLOUT1-	25	
AM20	TXLOUT1+	25	
AL21	TXLOUT2-	25	
AM21	TXLOUT2+	25	
AK18	TXLCLKOUT-	25	
AL18	TXLCLKOUT+	25	
AM18	TXLCLKOUT+	25	



RV410 MEMORY CHANNELS A and B

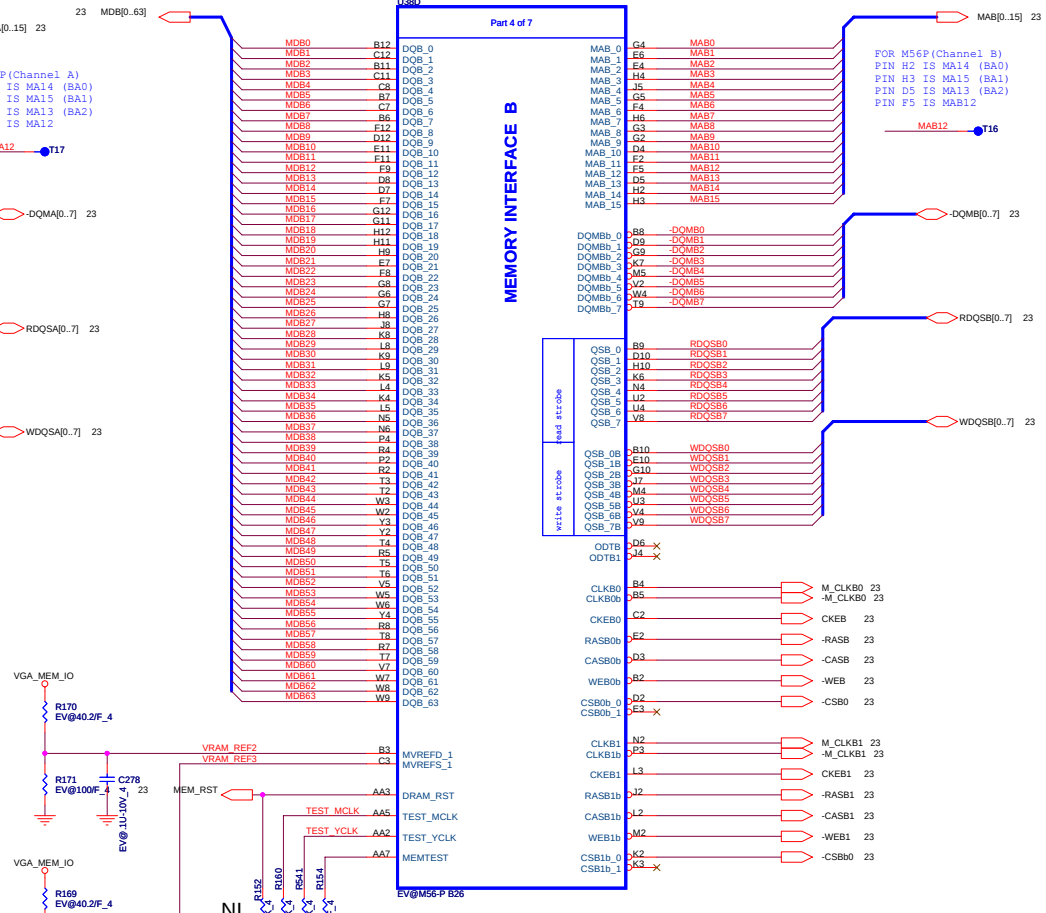
Channel A



Place VRAM_REF0, VRAM_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)
MVRREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVRREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

Channel B

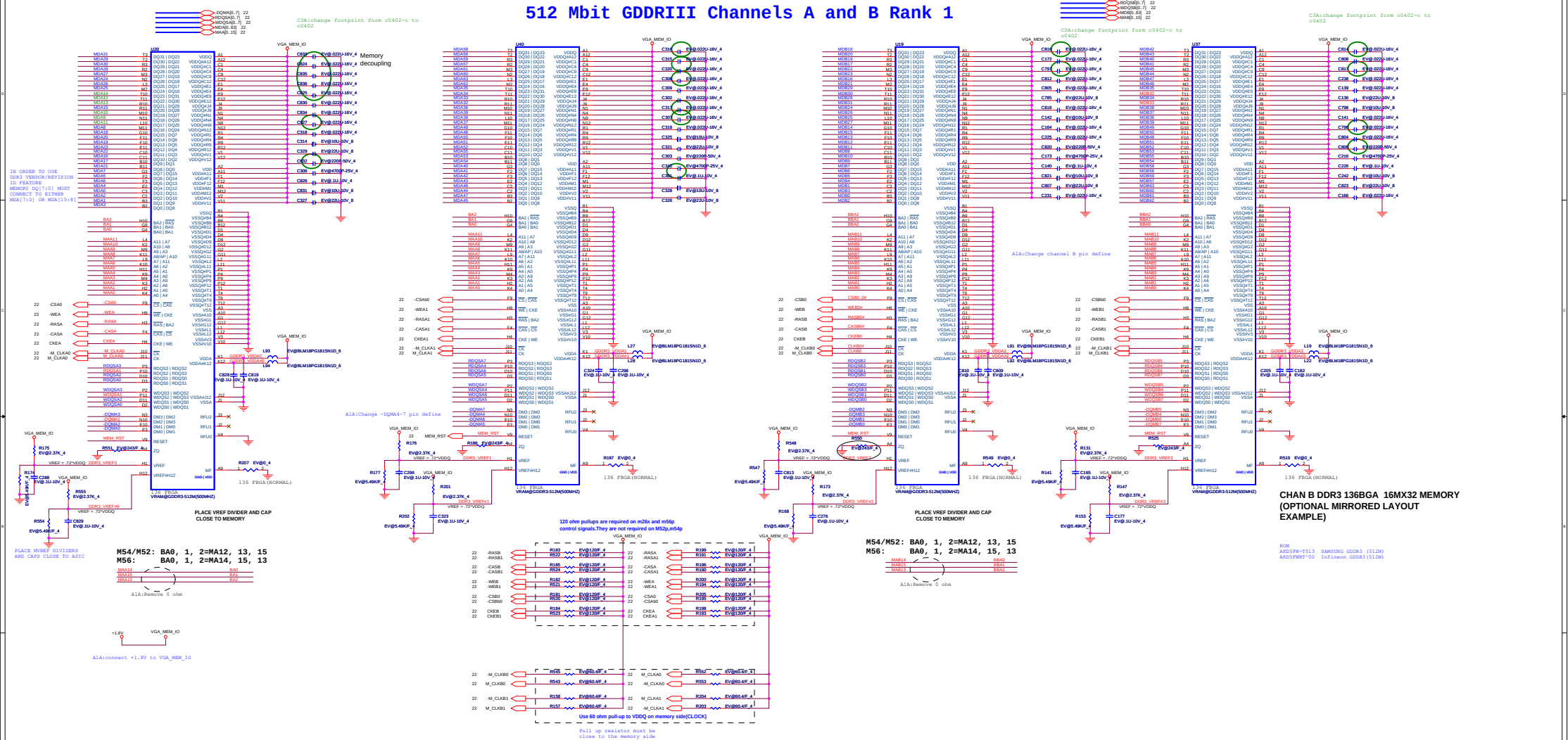


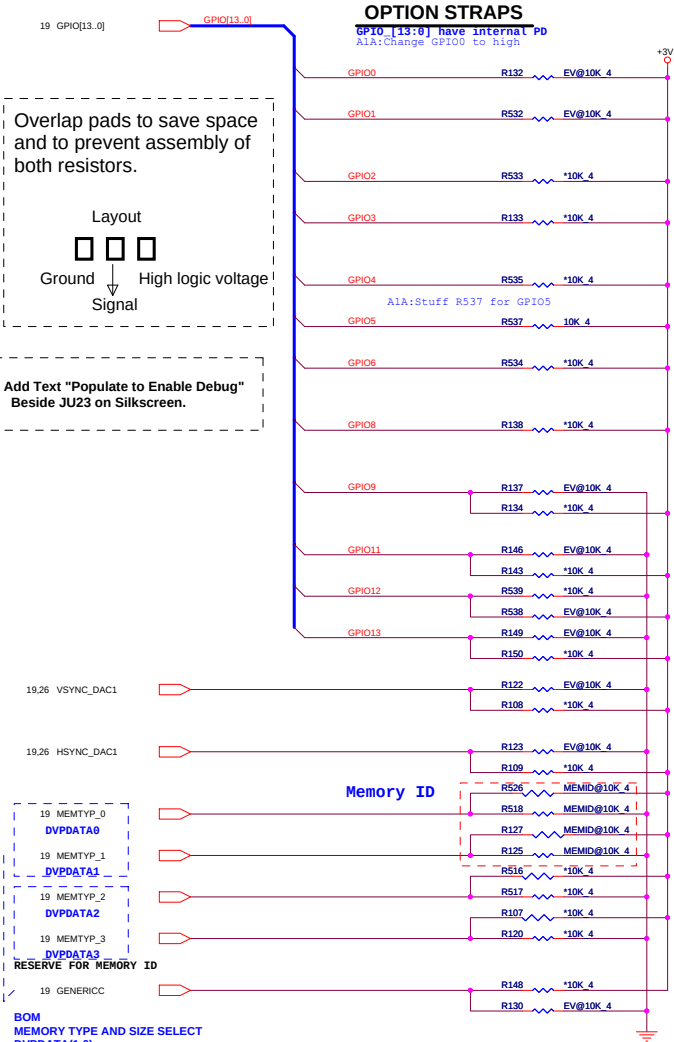
Reference voltage per channel (memory data/strobe)
MVRREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVRREFS_[0:1] (0.7 * VDDR1) (for GDDR3)



PROJECT : ZC3
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512 Mbit GDDRIII Channels A and B Rank 1





M56-P Strap

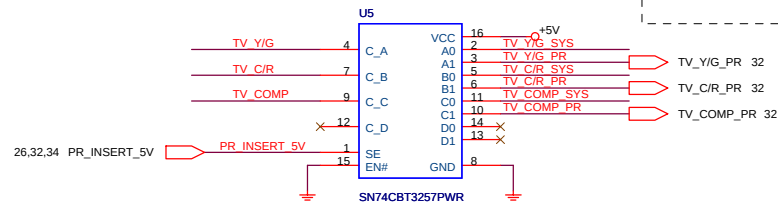
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26,M50P: INSTALL WITH ATT R8450,R8450D,RX450, RC410,R8452 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M2X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9:13:11)	IF NO ROM GPIO11(M26X) AND GPIO12.13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=0(128MB) 001x - No ROM, MEM_AP_SIZE=01(256MB) 010x - No Rom, MEM_AP_SIZE=10(512MB) 011x - No ROM, MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDs from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present, 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	H2SYNC	RSVD	
	PCIE_TEST	RSVD	

Board Straps		REV. 0.3	
STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVPDATA(1:0)	MEMORY TYPE AND SIZE SELECT->DVPDATA(1:0) 00 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 01 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Hynix GDDR 3 memory(512Mb) 136 Ball BGA package 11 - Reserved	00
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Not detected	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1

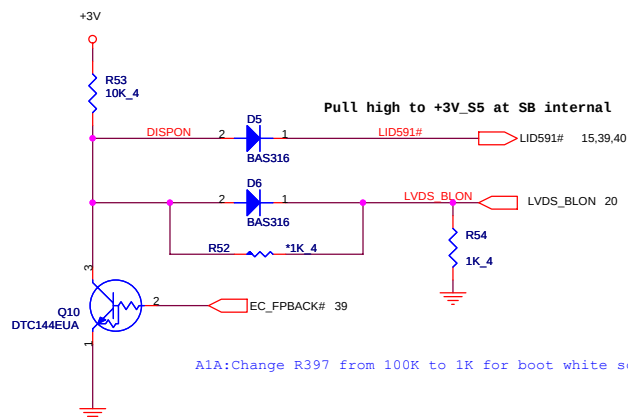
S-VIDEO

TV Out (SVHS) MiniDIN 7-pin

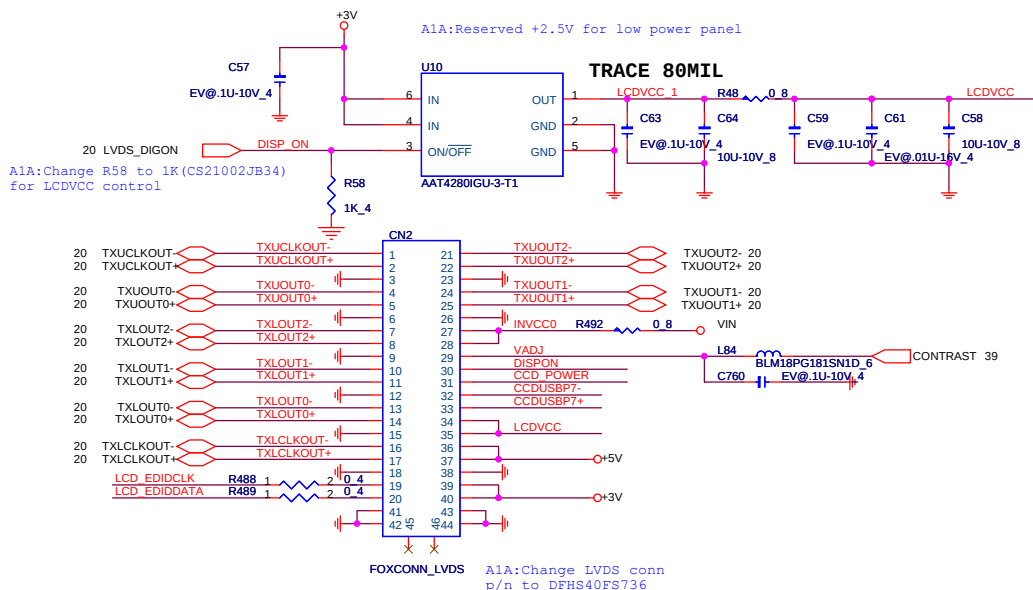
A1A:Change R1,R3,R6 to 150 ohm for TV can't detect issue



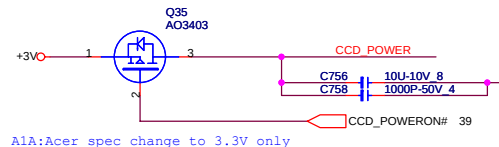
A1A:Change to SN74CBT3257PWR (Vin 5V)



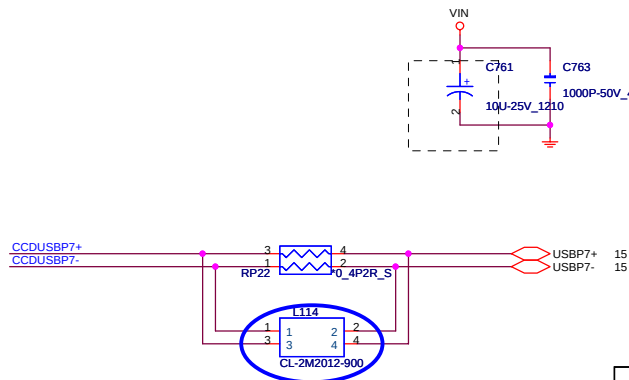
A1A:Change R397 from 100K to 1K for boot white screen issue



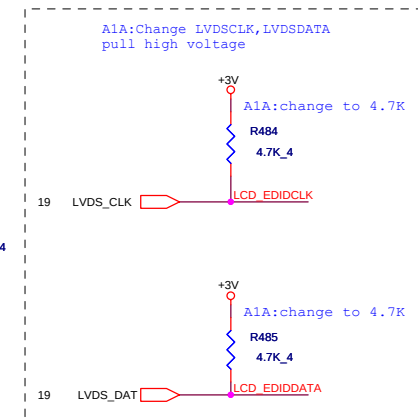
CAMERA MODULE CONNECTOR

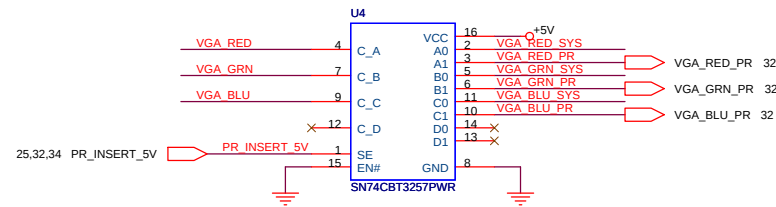
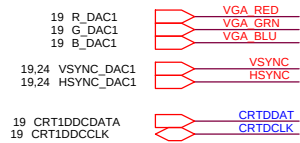


A1A:Acer spec change to 3.3V only



C3A:
change EMI FILTER to CL-2M2012-900JT for EMI request



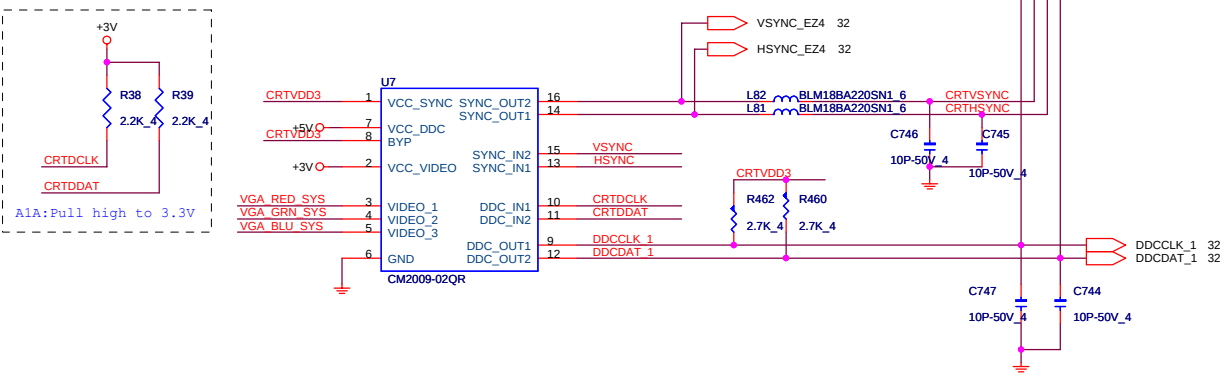
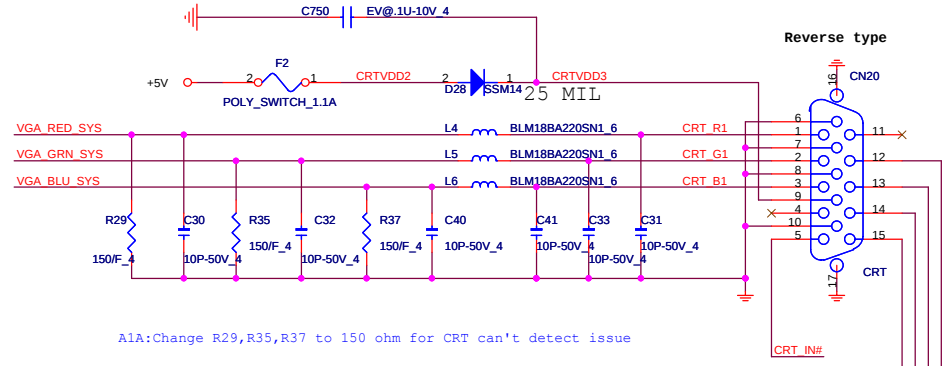
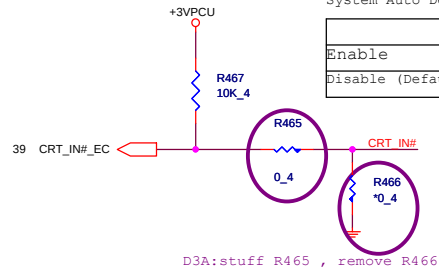


A1A:Change to SN74CBT3257PWR (Vin 5V)

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

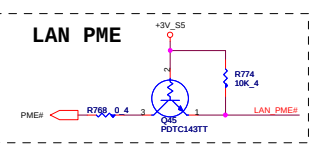
System Auto Detect External CRT Device

	R7059	R7058	R27
Enable	Not stuffed	Stuffed	Stuffed
Disable (Default)	Stuffed	Not stuffed	Stuffed

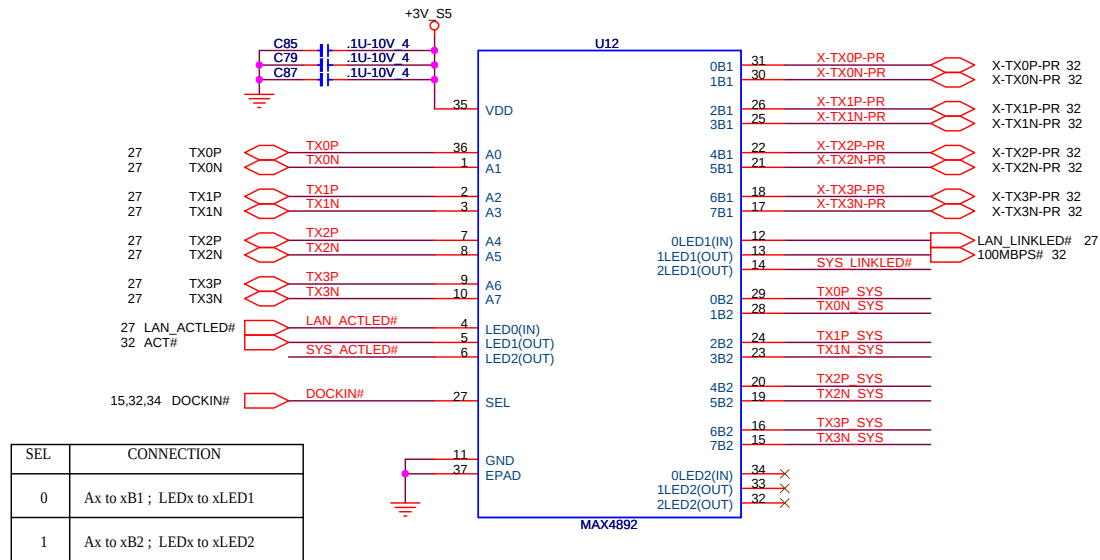


PROJECT : ZC3
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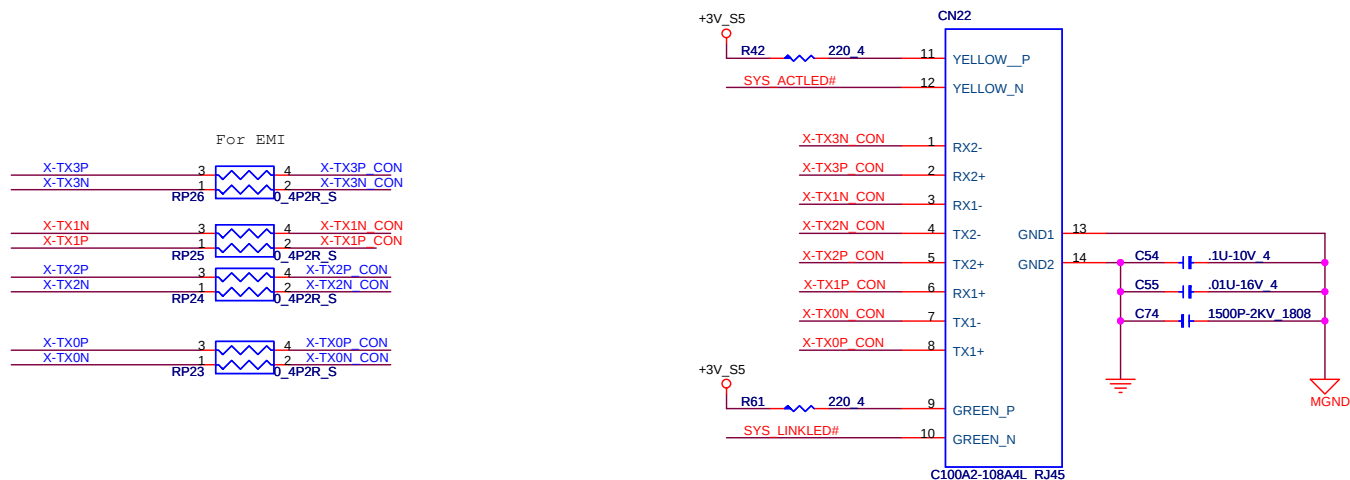
LAN
BCM5787MKFBG :
AD20 REQ2#
GNT2# INTF#



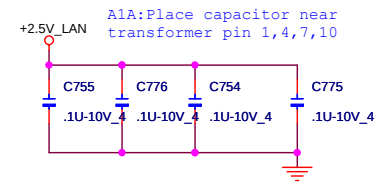
PROJECT : ZC3 Quanta Computer Inc.		
Size	Document Number BCM5788MG LAN	Rev 1A
Date:	Thursday, June 08, 2005	Sheet 27 of 46



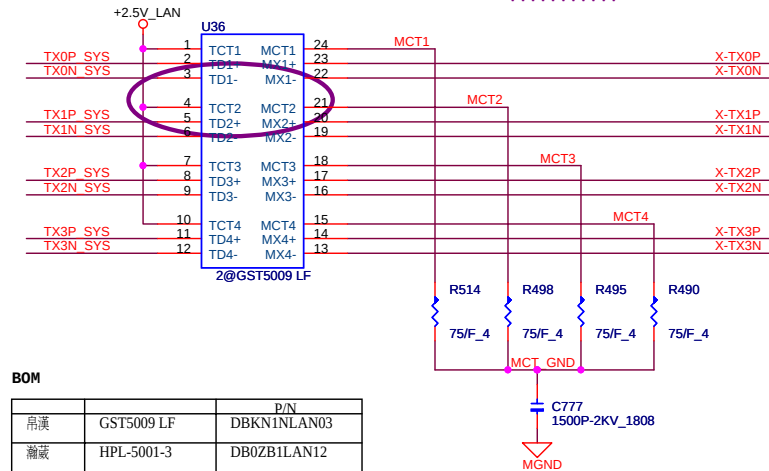
A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



A1A:Add diode for 10/100M
& 1000M led control

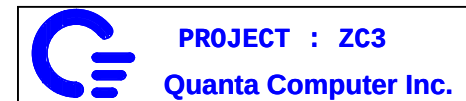


D3A:change transformer to meet IEEE test, update to ???????????



BOM

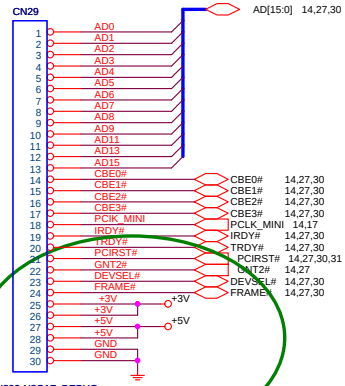
		P/N
吊漢	GST5009 LF	DBKN1NLAN03
蕭漢	HPL-5001-3	DB0ZB1LAN12



Size	Document Number	Rev
	TRANSFORMER/RJ45	1A
Date:	Thursday, June 08, 2006	Sheet 28 of 46

Debug card interface

BOT contact

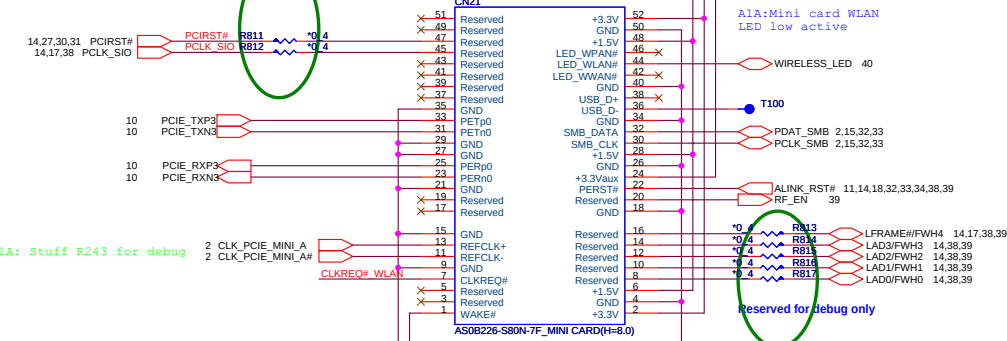


C3A:remove PCI debug conn

*AF:800-N2G12_DEBUG

B1A:These signals of reserve have be used by wireless module of Foxconn BG. These signals impact LPC, I remove signal line in order to solve the WLAN issue.

Reserved for debug only



B1A: Stuff R243 for debug



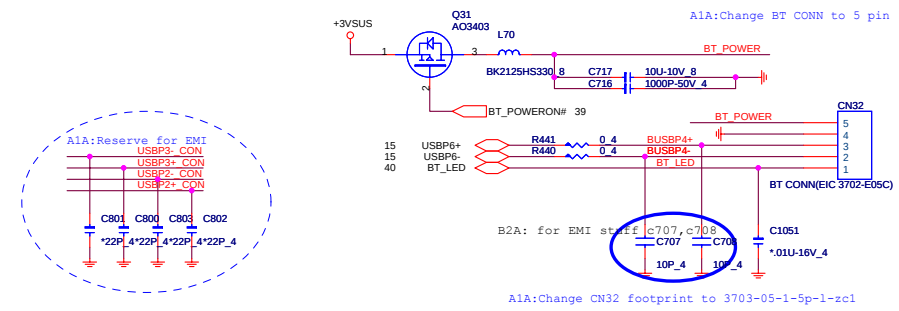
B2A:Add R799,R800,R801,R802,R803,R804,R805 for debug port,place on uder CN21(BOT)



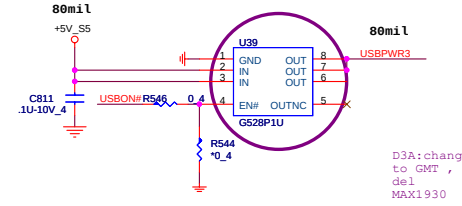
CLKREQ# and WAKE# are open drain signal



BLUETOOTH MODULE CONNECTOR

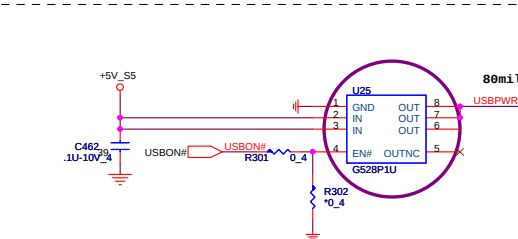
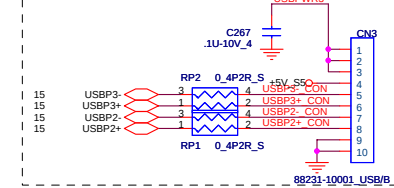


A1A:In adapter mode, should be powered during S0-S5.
In battery only mode, should be powered during S0 and S3, and not powered during S5

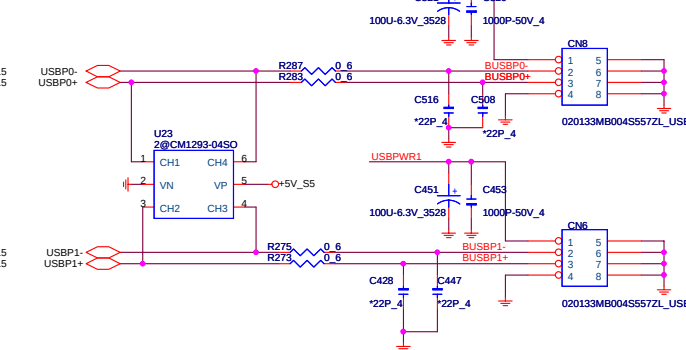


MB USB PORT(REAR)

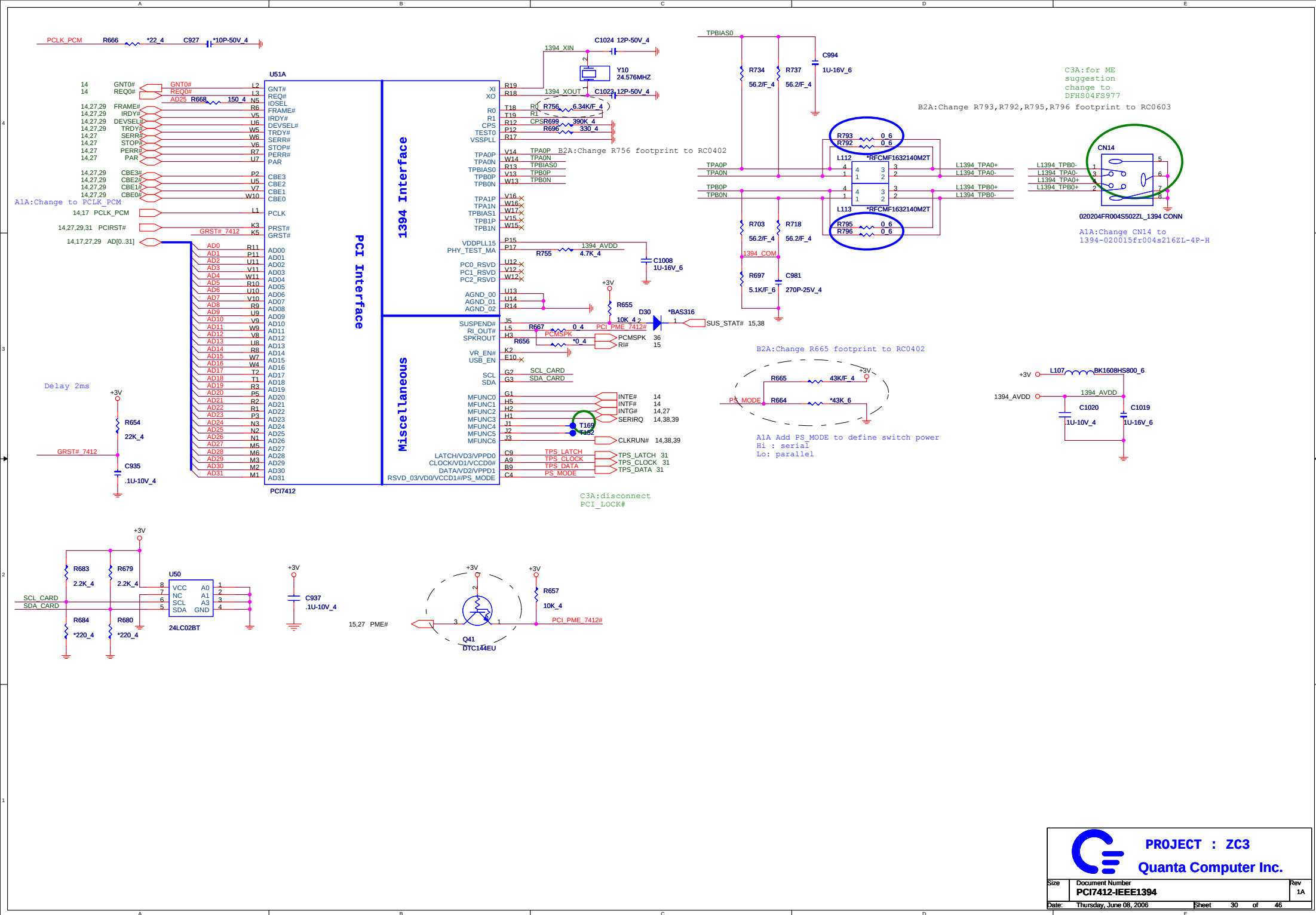
A1A:Change CN3 pin 4 to +5V_S5

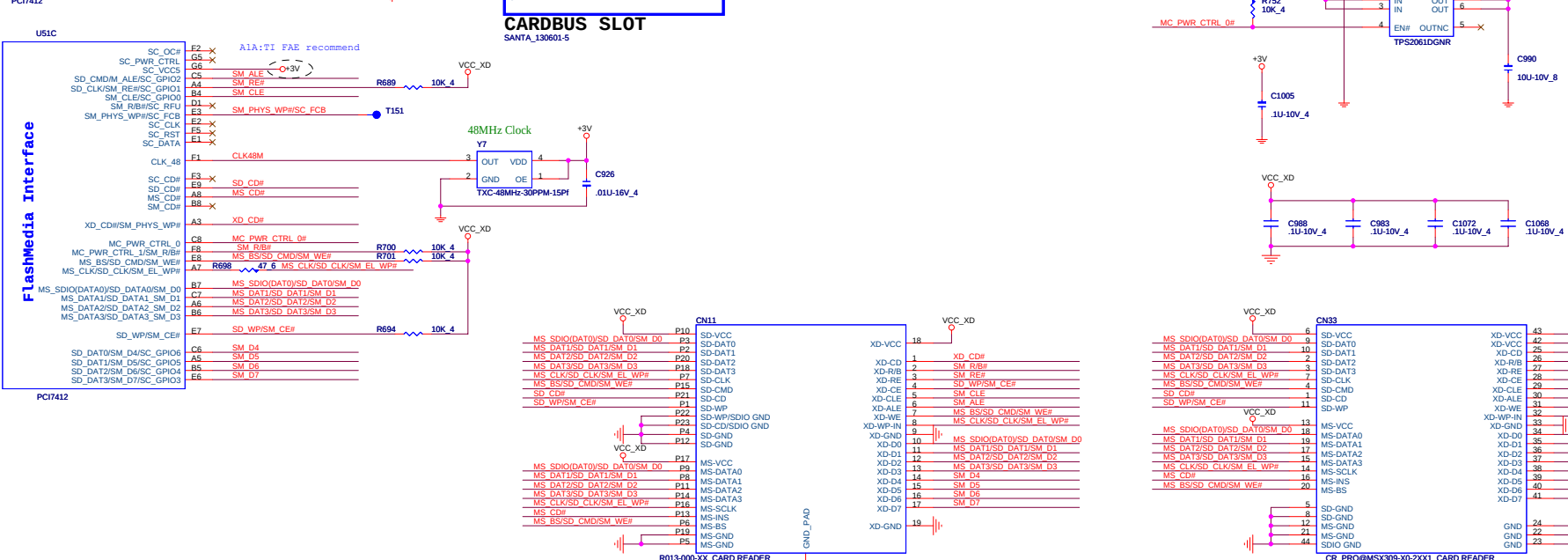
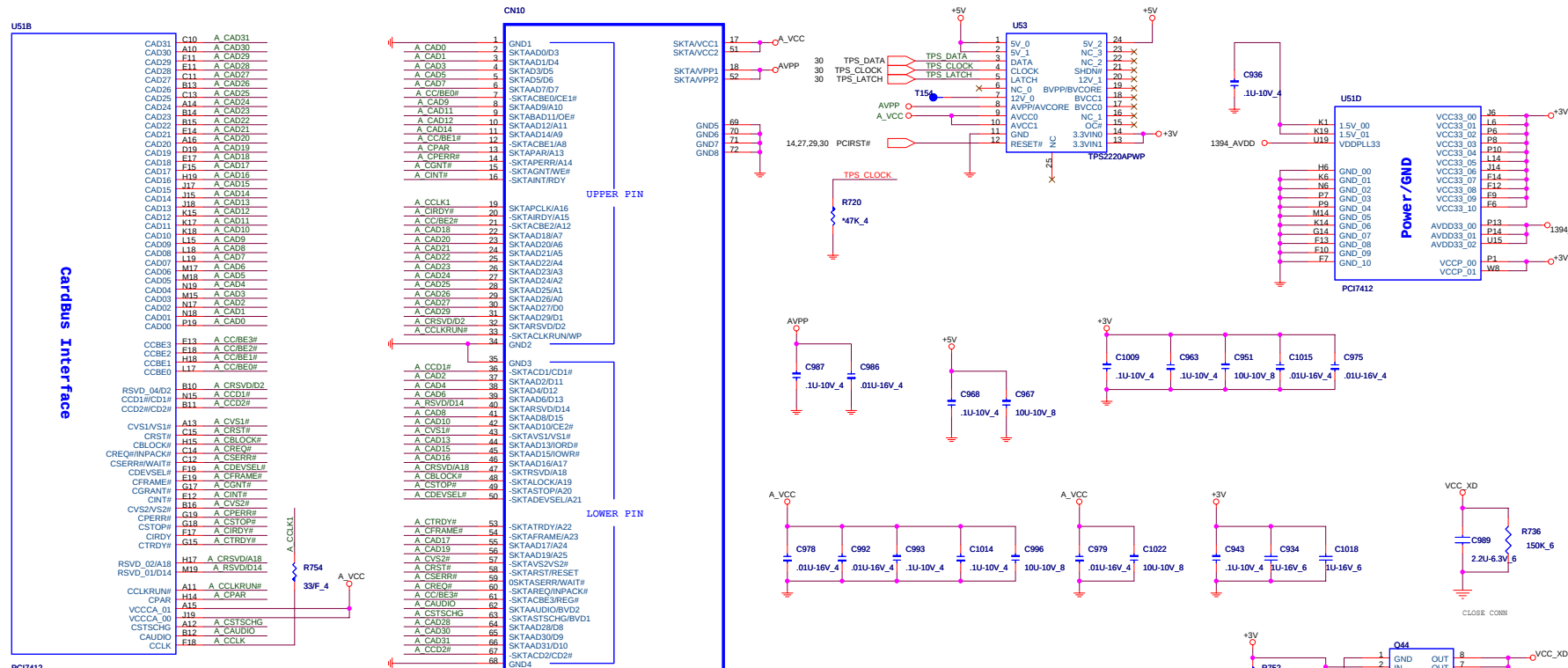


MB USB PORT (RIGHT)



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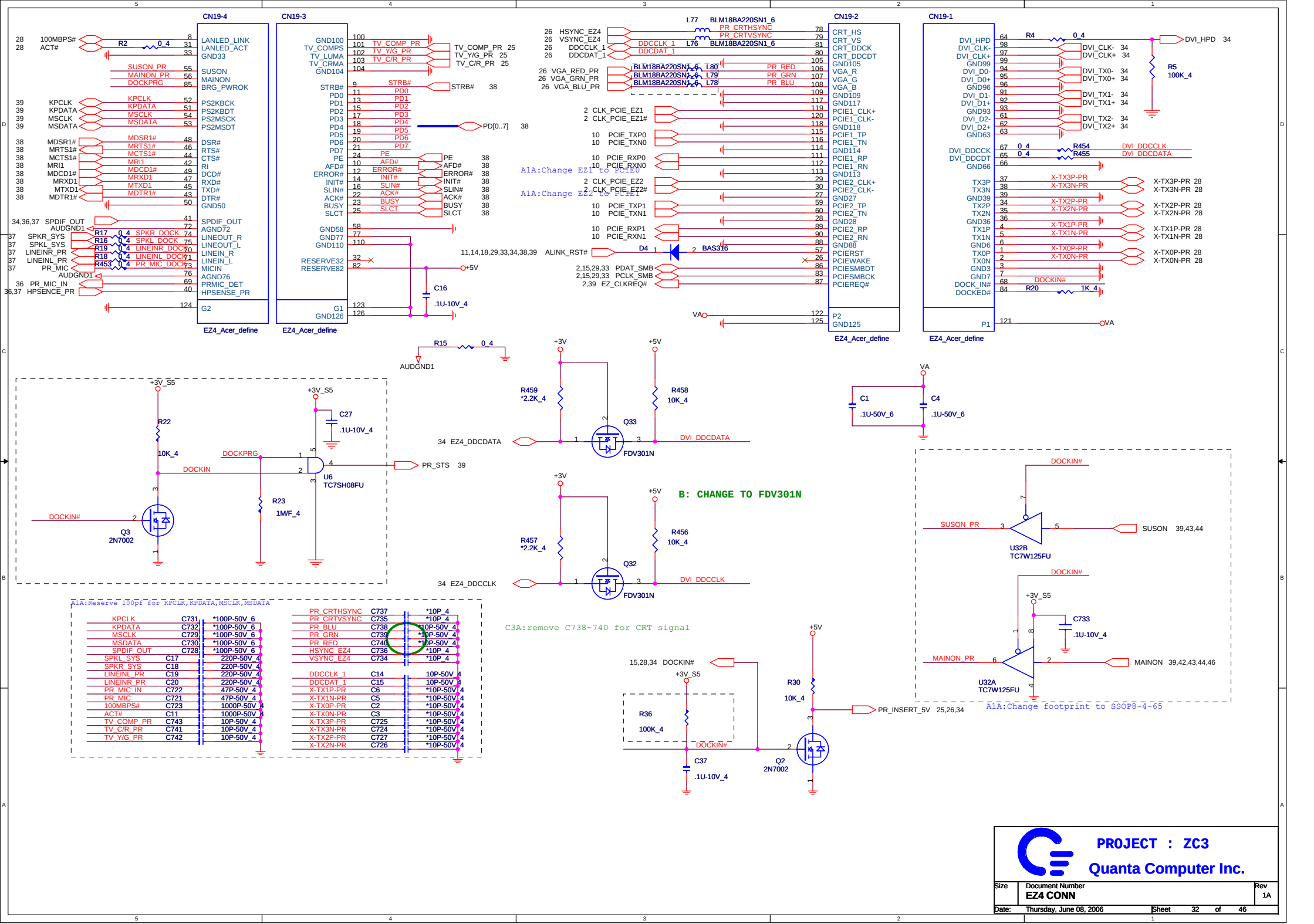




5 IN1 CARD READER



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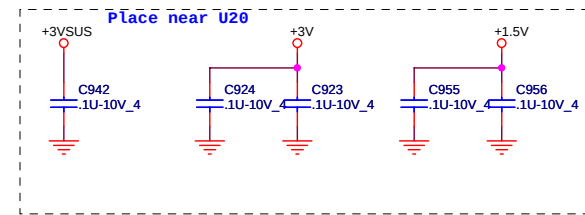
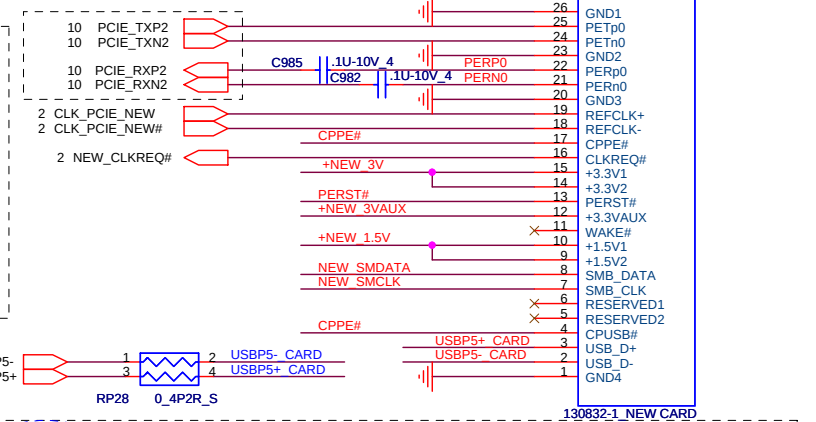
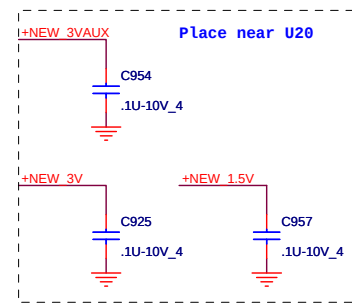
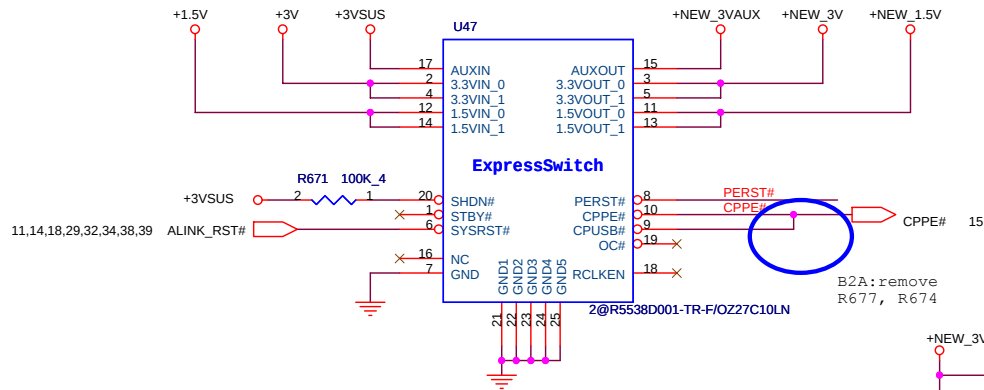


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+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

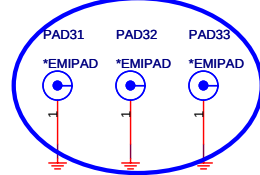
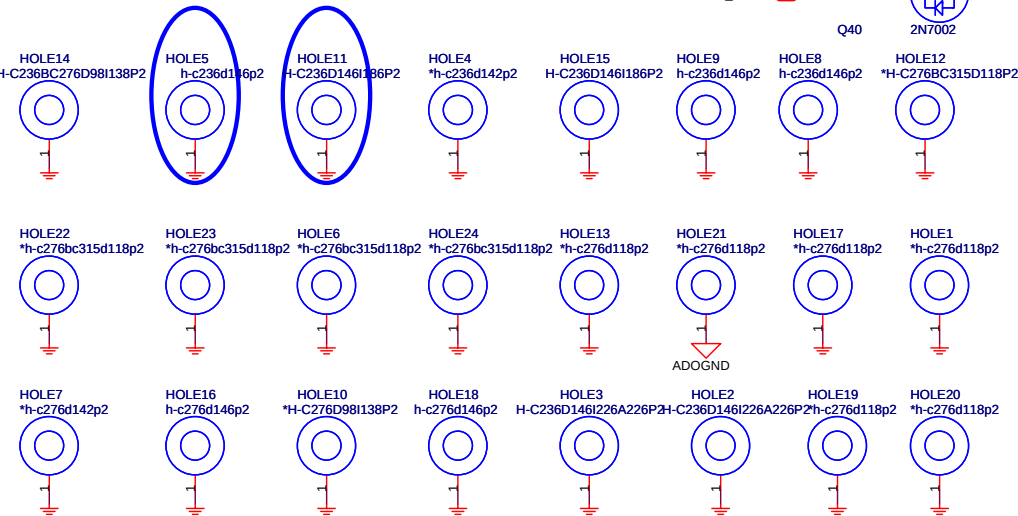
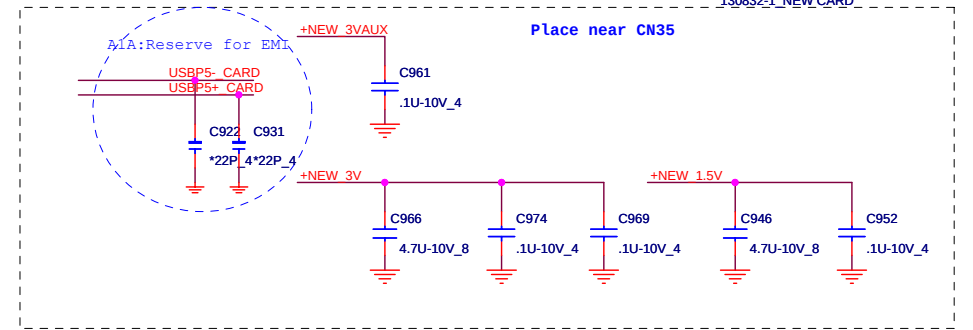
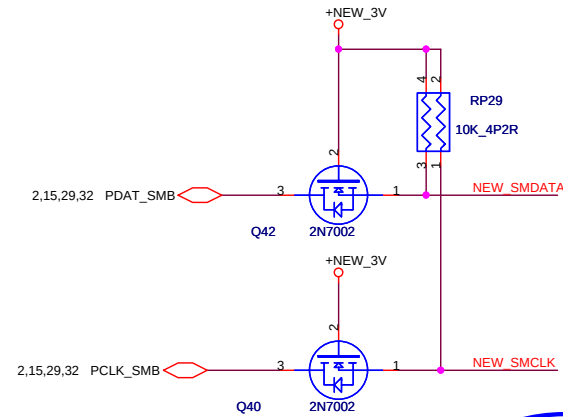
A1A:Change New card power sw to Oz27c10

A1A:Change New card to small type(130832-1)
Reverse

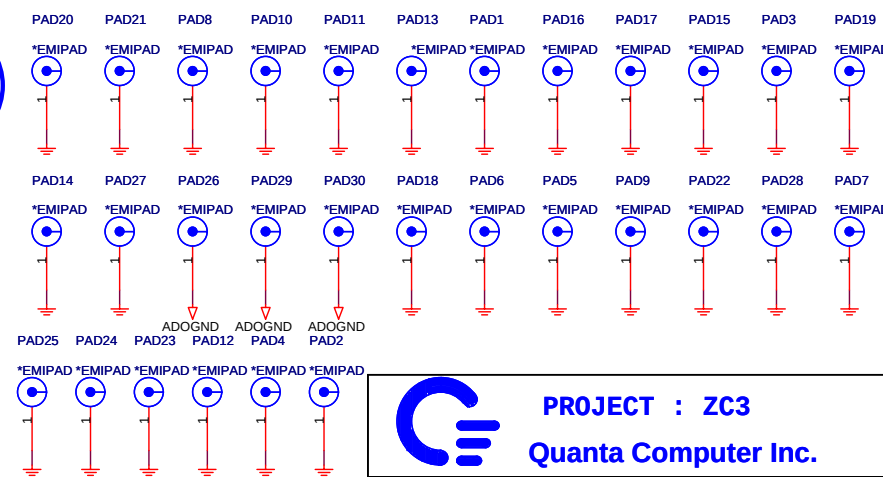


B2A:update footprint to h-c236d146p2

B2A:update footprint to H-C236D146I186P2



B2A:MB-IR-SUP-BKT-ZC1



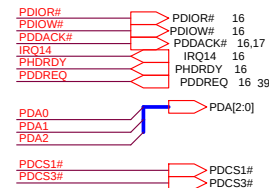
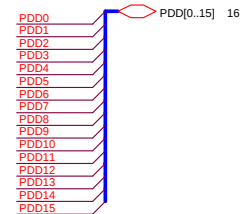


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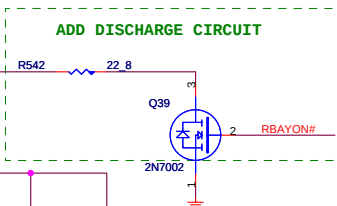
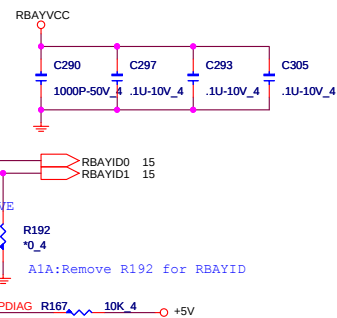
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	NEW CARD & HOLE	1A
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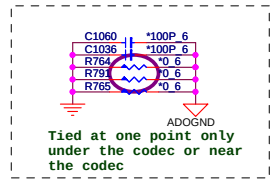
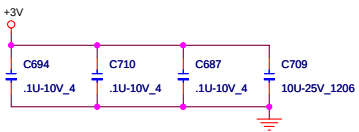
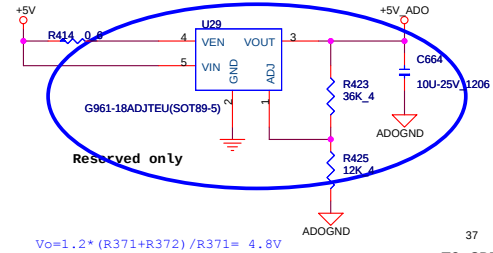
RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD



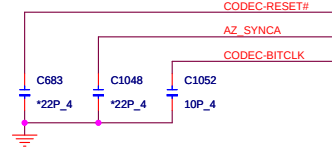
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B2A: for audio noise
del
L55,C657,C661,C1063,C675,C679,C1064
stuff U29,R414,R423,R425,C664

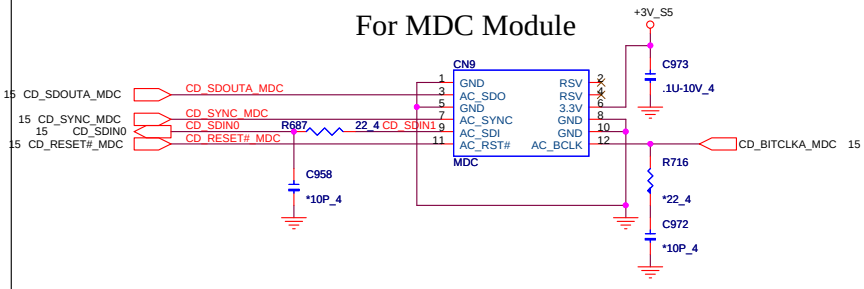
Option of External Volume
Control or Standby
Mode/De-Pop



D3A:remove R791



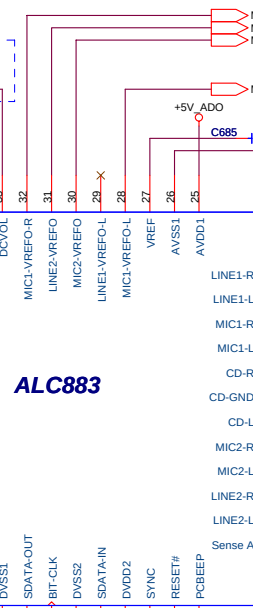
For MDC Module



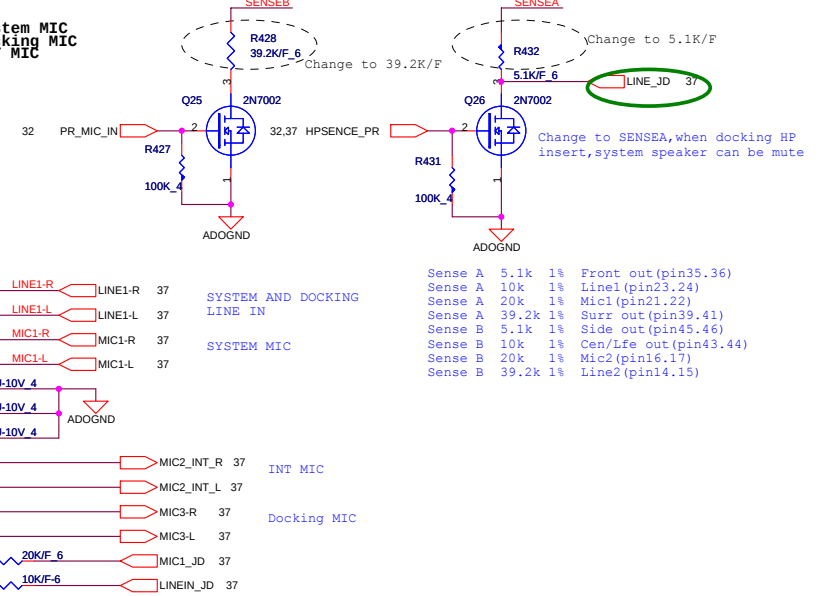
TO Headphone AMP

TO SPEAKER AMP

ALC883



System MIC Docking MIC INT MIC



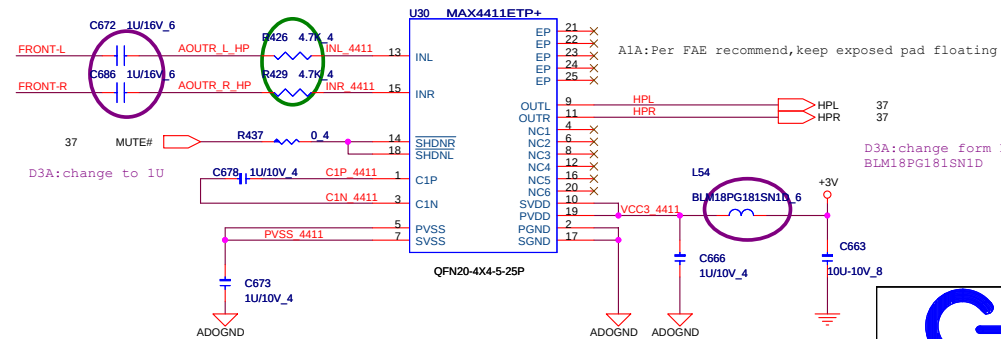
Sense A	5.1k	1%	Front out (pin35.36)
Sense A	10k	1%	Line1 (pin23.24)
Sense A	20k	1%	Mic1 (pin21.22)
Sense A	39.2k	1%	Surr out (pin39.41)
Sense B	5.1k	1%	Side out (pin45.46)
Sense B	10k	1%	Sen/Lfe out (pin43.44)
Sense B	20k	1%	Mic2 (pin16.17)
Sense B	39.2k	1%	Line2 (pin14.15)

A1A:Change AZ_SDIN1 series resistor from 33 to 22 ohm

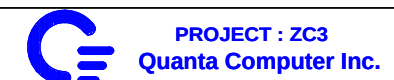
Change from 1UF to 4.7UF to meet vista performance requirement

C3A:change 0 to 4.7k to avoid noise

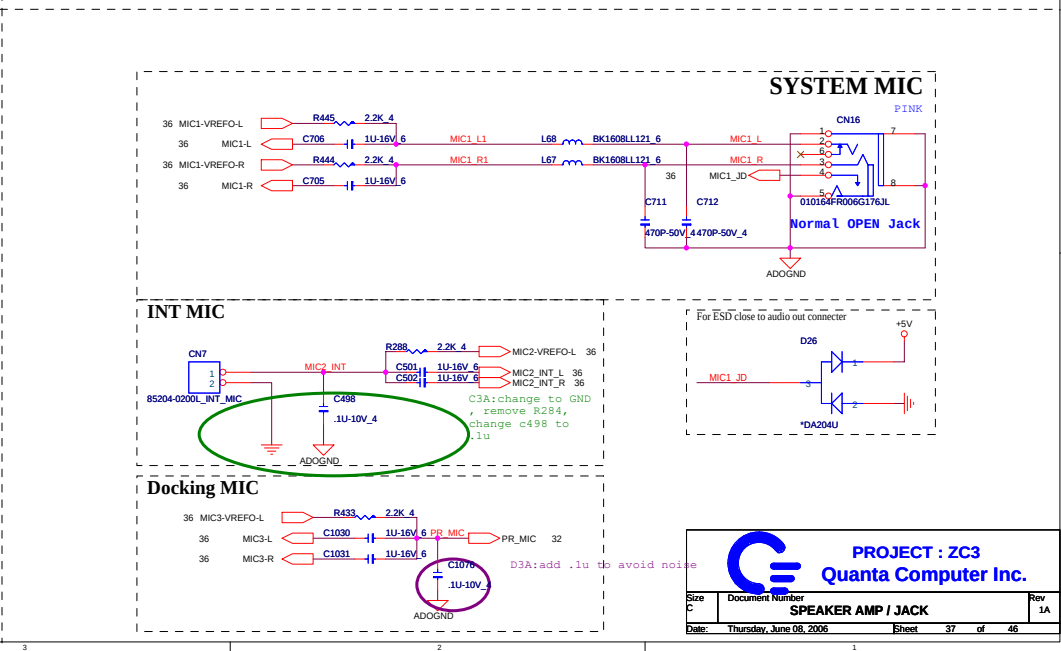
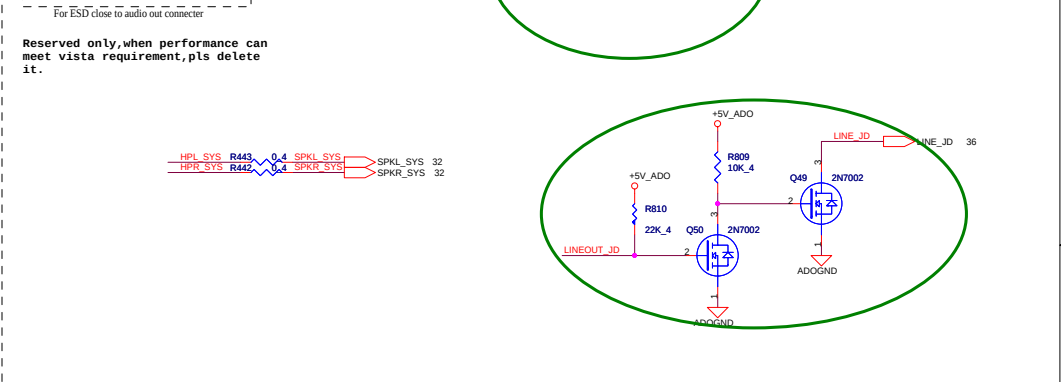
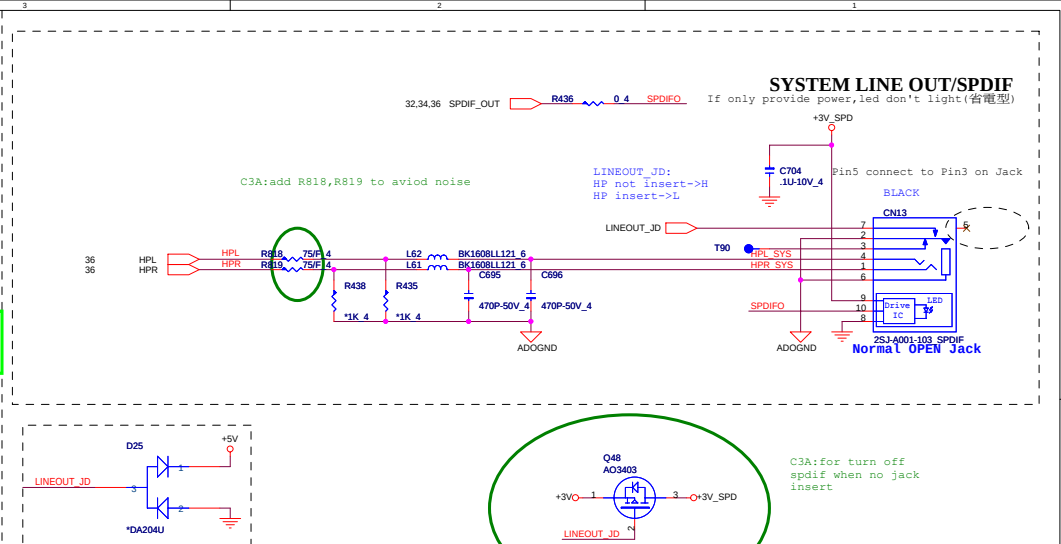
Headphone Amplifier

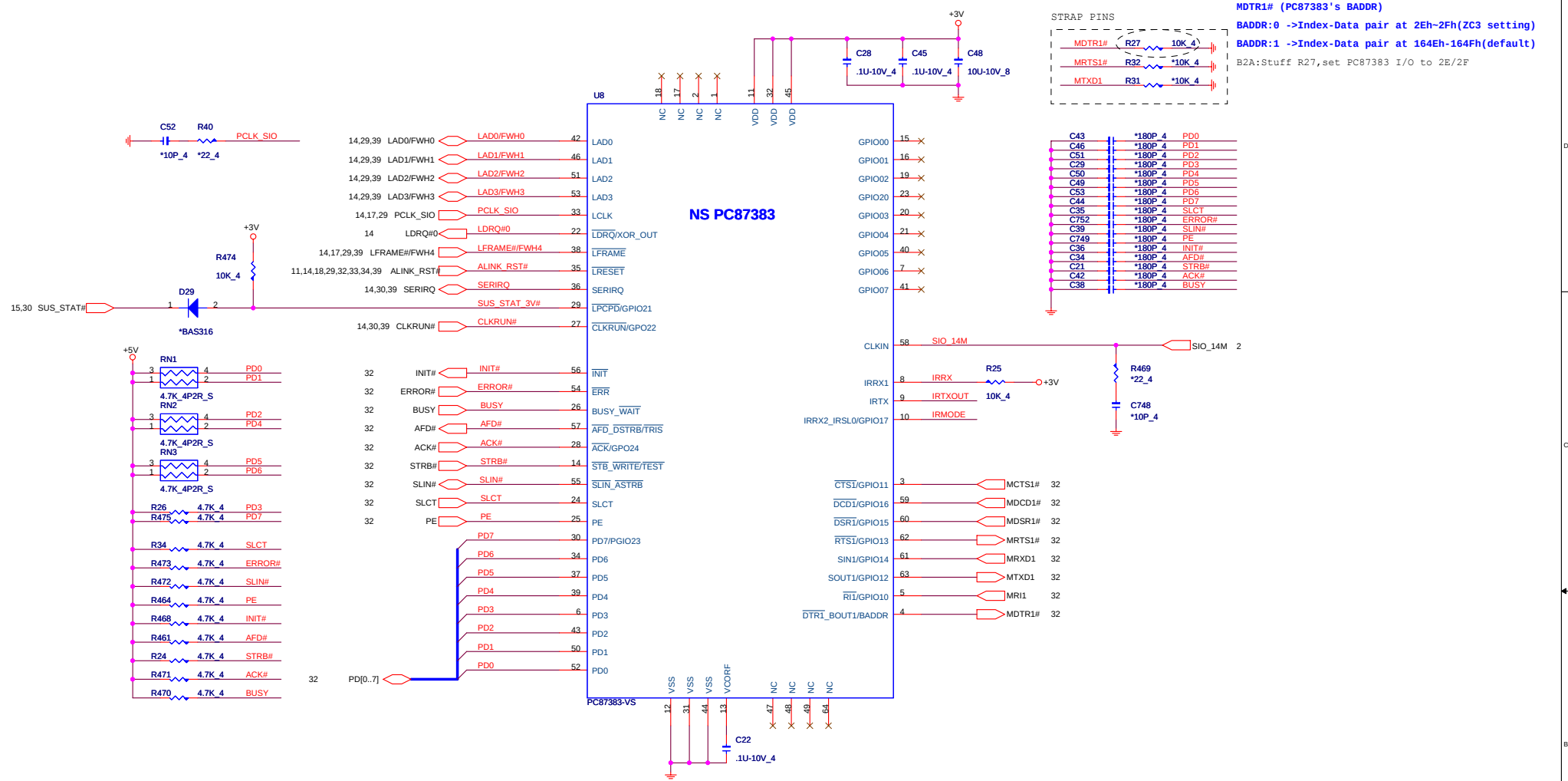


D3A:change form BLM11A601S to BLM18PG181SN1D

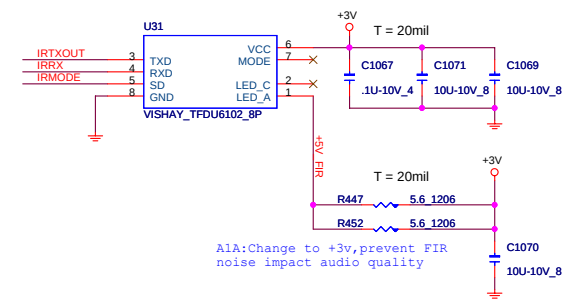


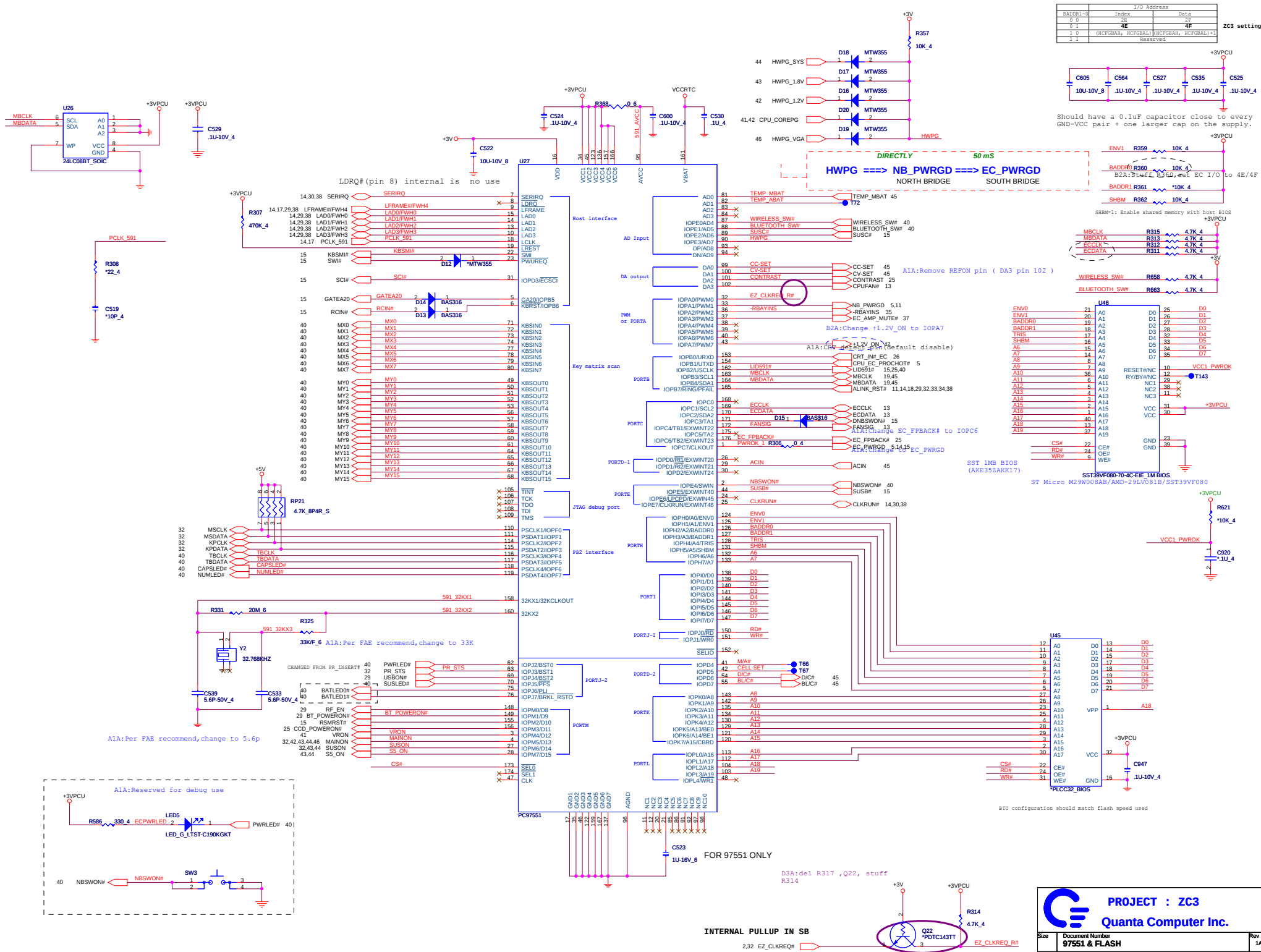
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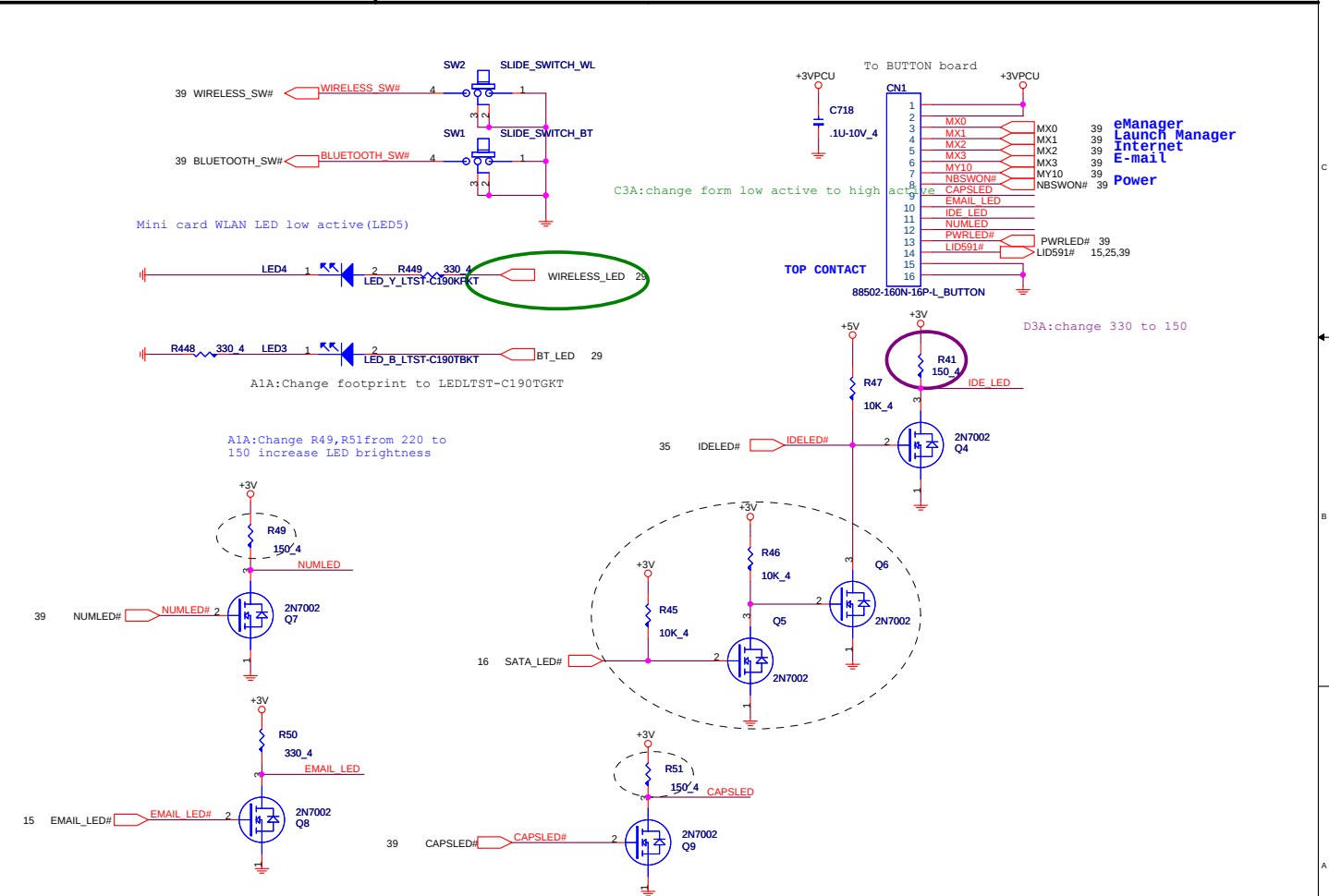
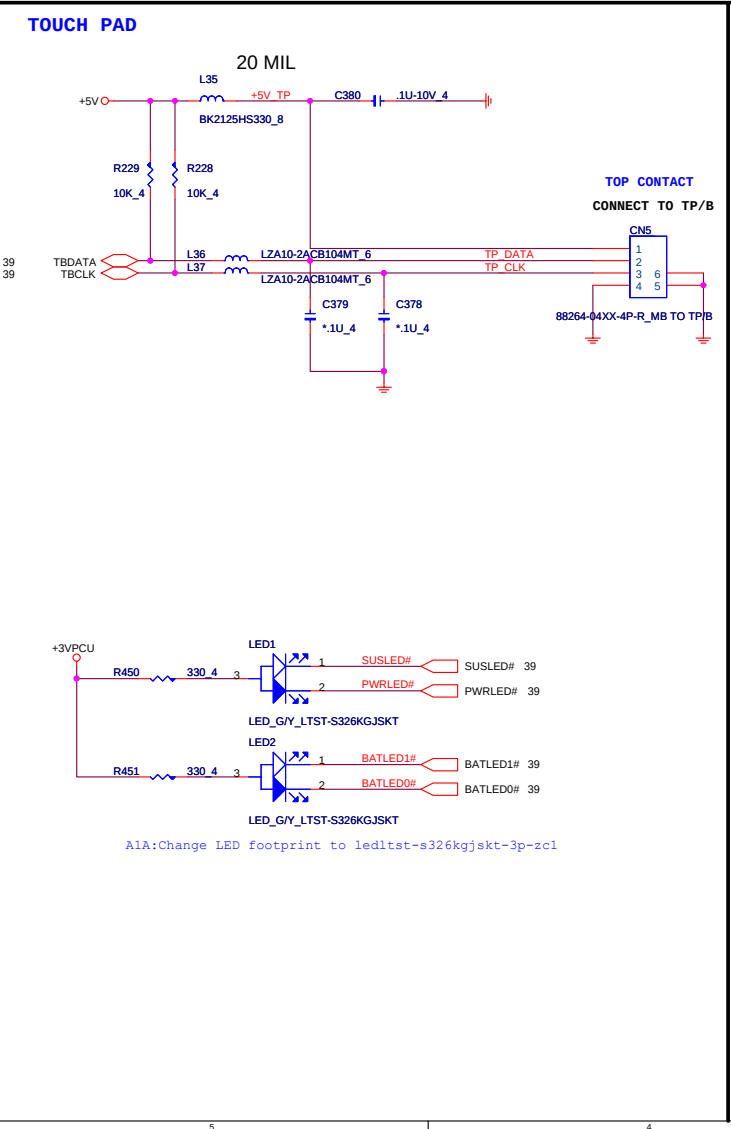
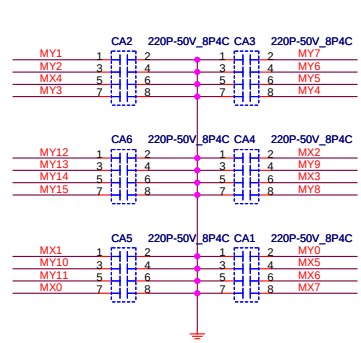
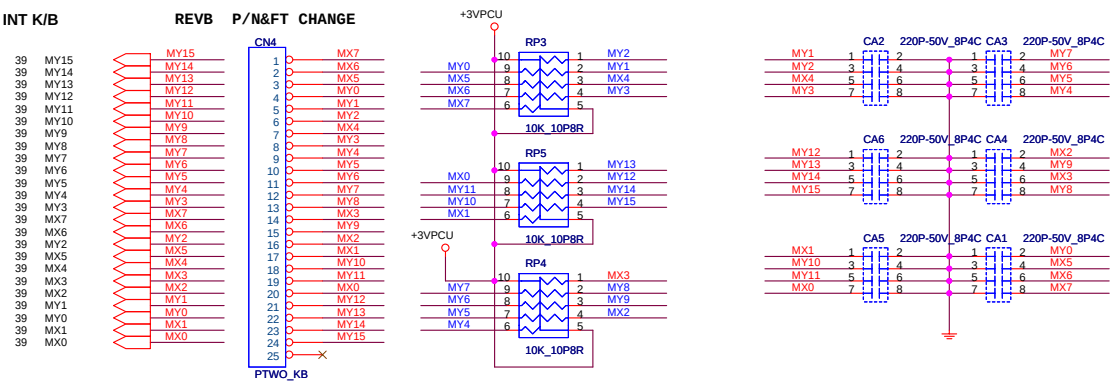


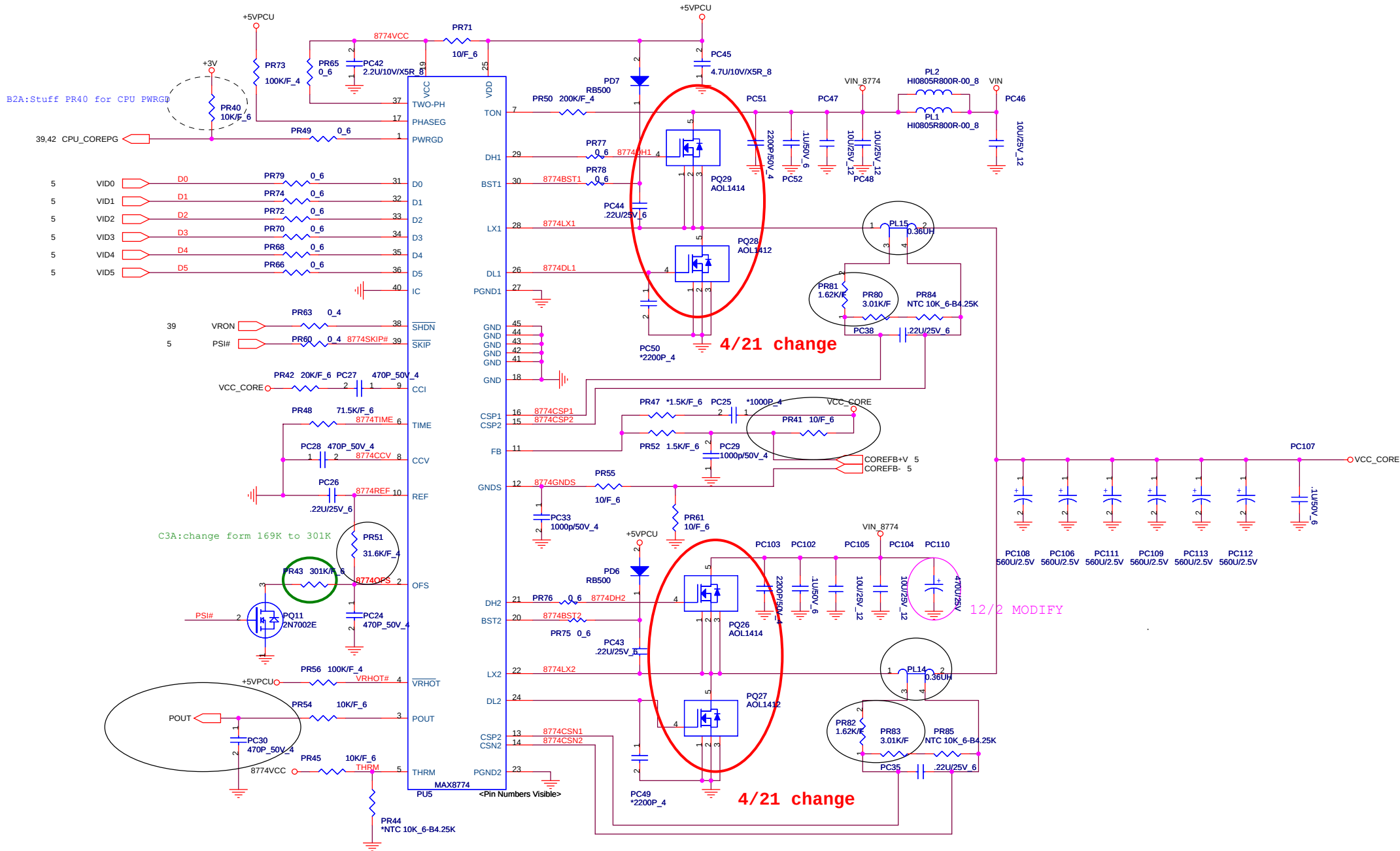


FIR





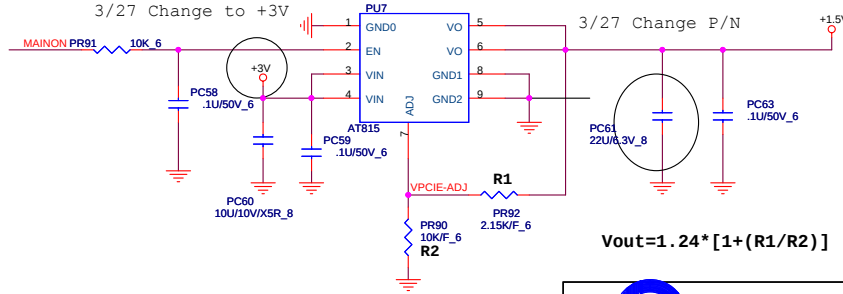
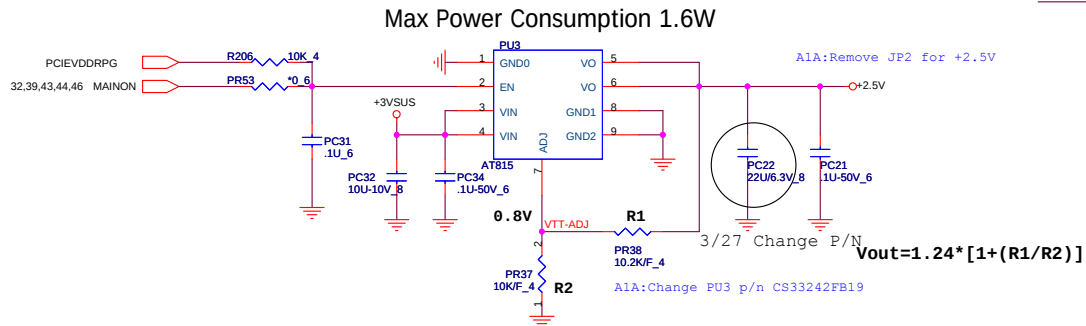
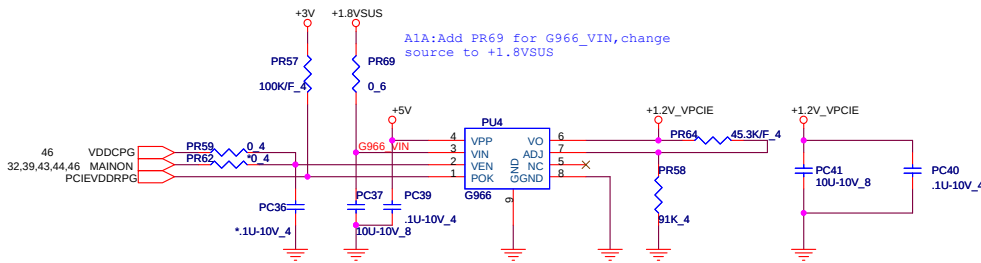
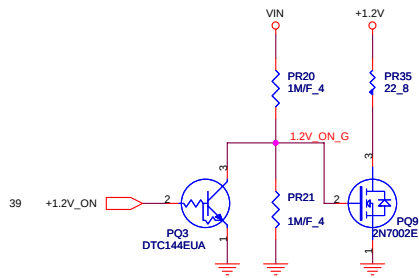
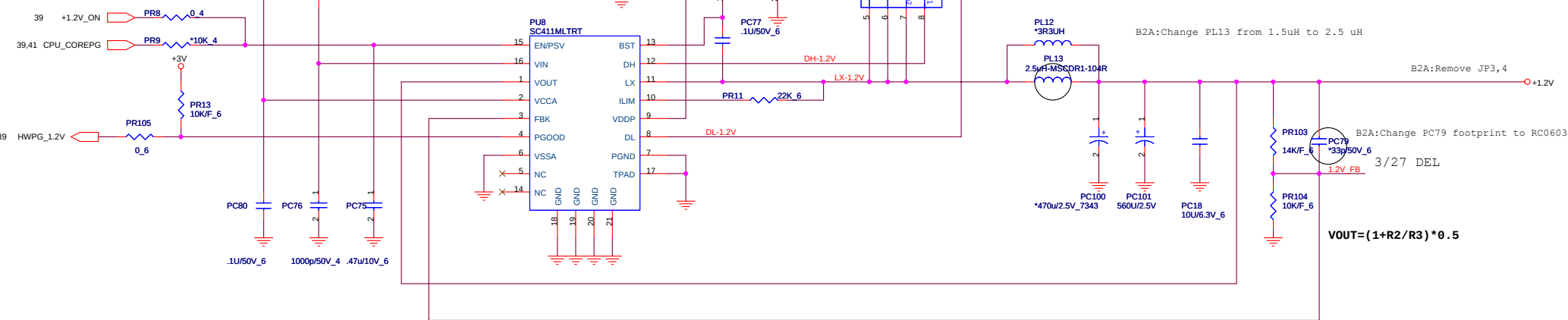


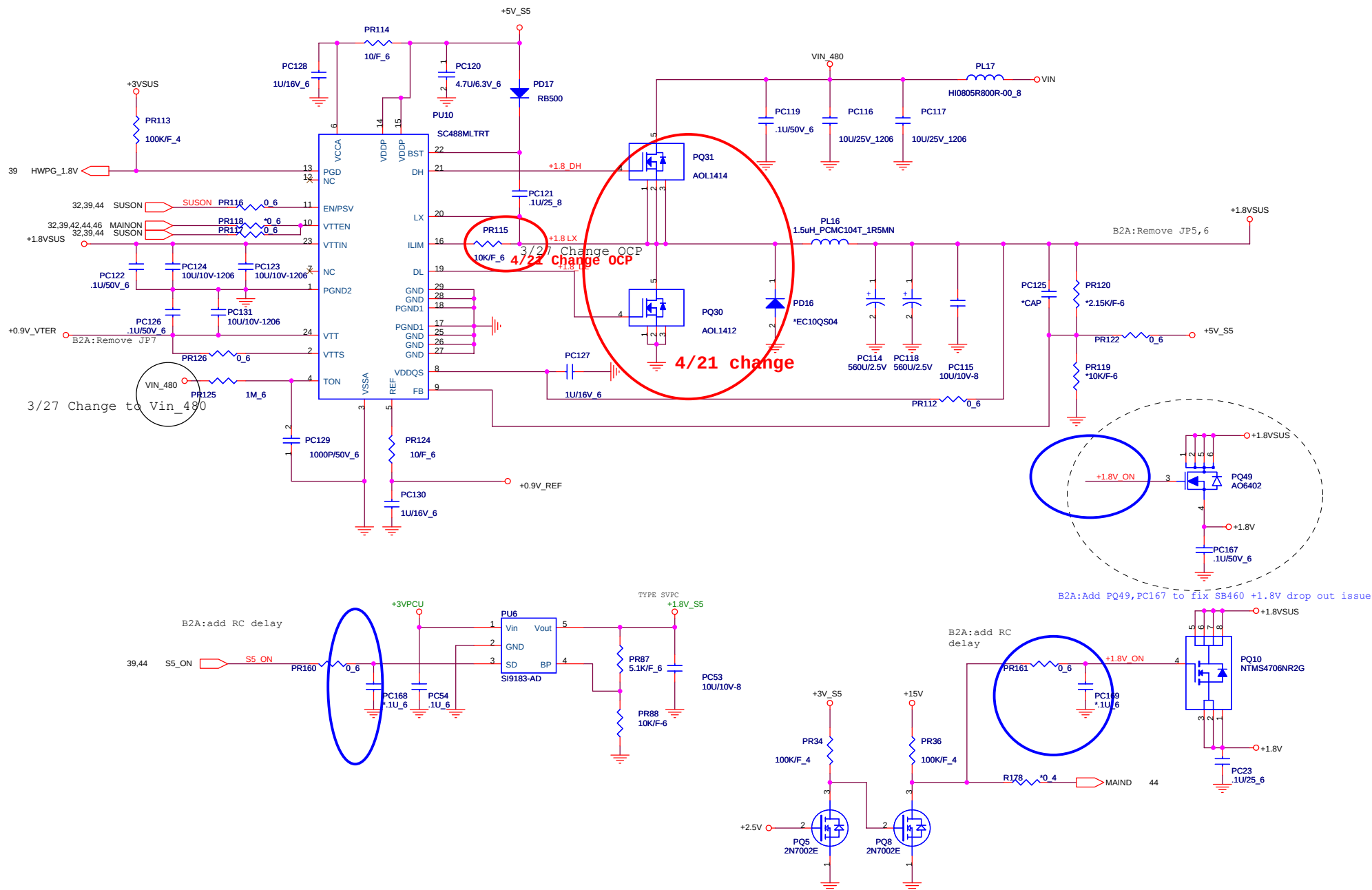


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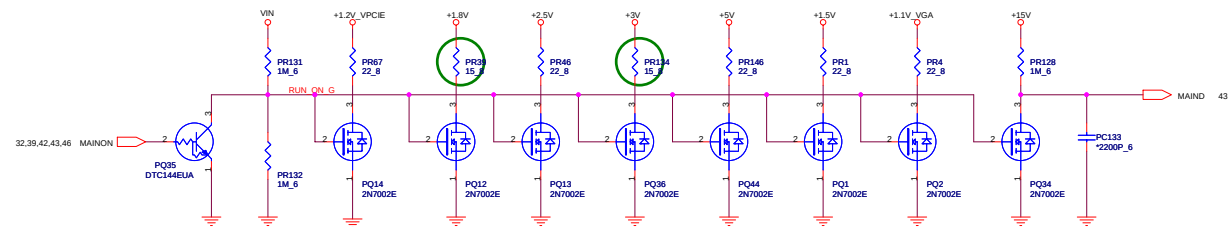
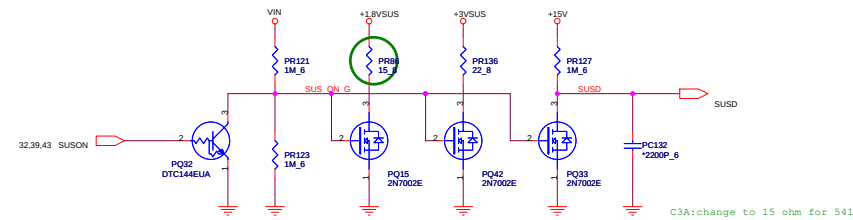
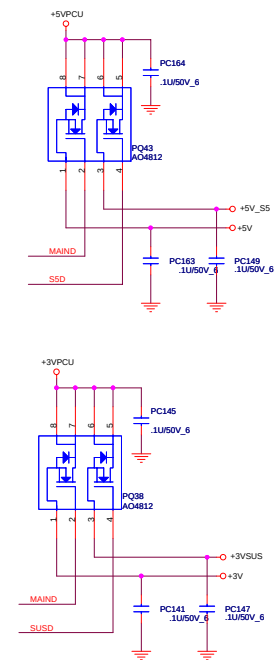
AMD power sequence:
VDDIO (+1.8VSUS), VTT (+0.9V VTER), VDD
(CPU core power), and VLDI (+1.2V)

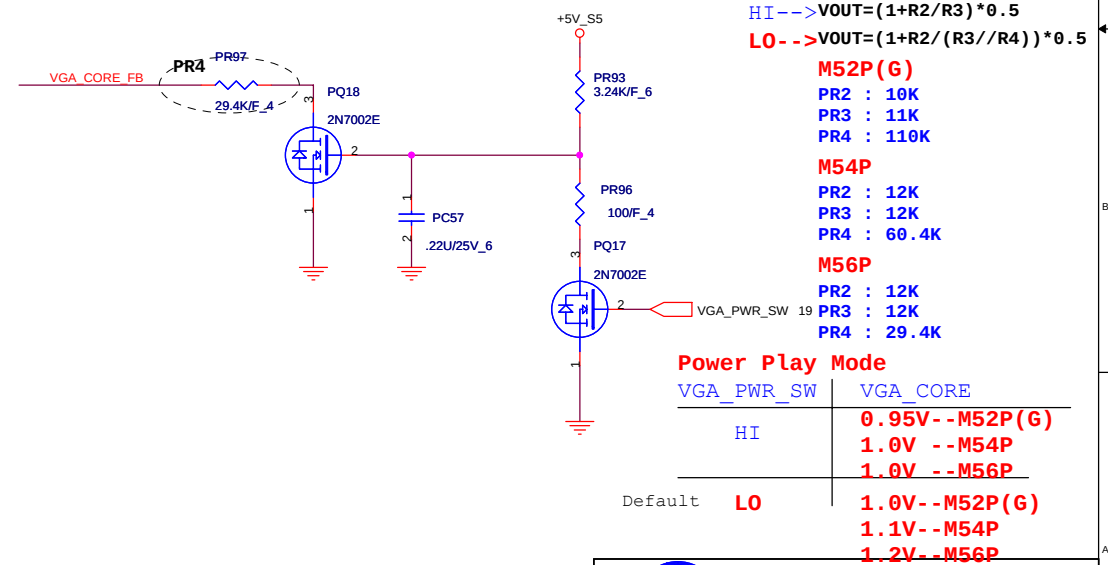
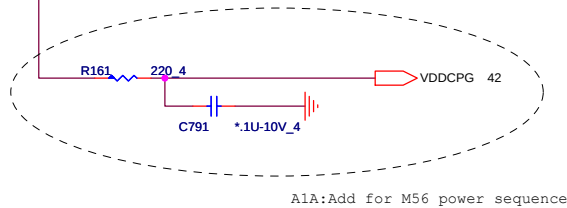
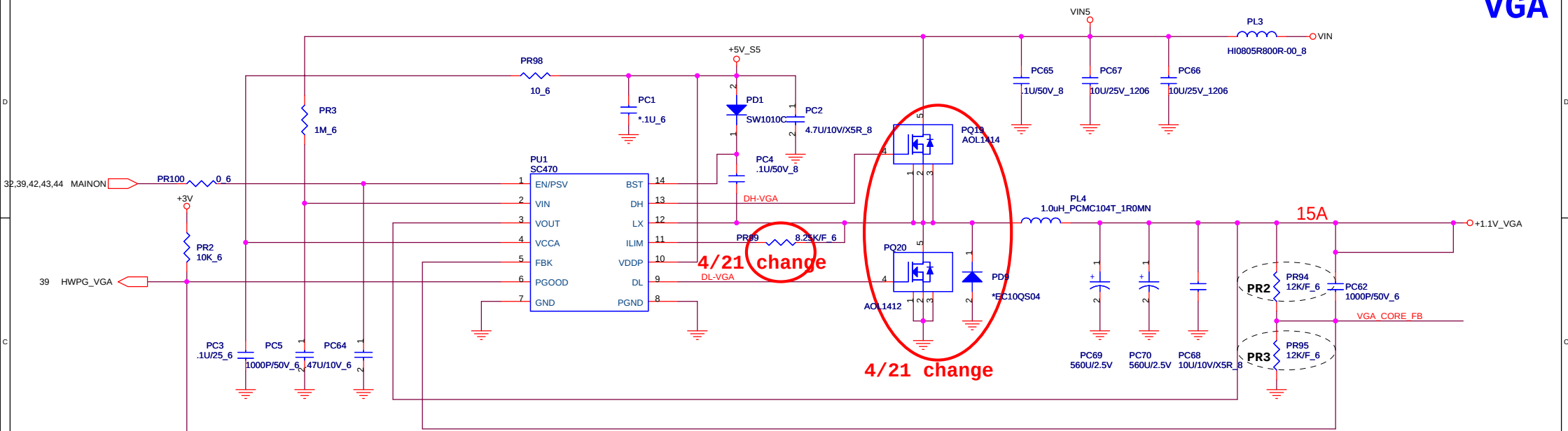




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